IBM Field Engineering

Maintenance Diagrams

2020 Processing Unit

System/360 Model 20

(Machines with serial no. 50,000 and above)

Volume 2

SY33-1042-1

This publication (Volume 2) and its companion publication (Volume 1, Form Y33-1024) constitute the Field Engineering Maintenance Diagrams manual for the IBM 2020 Processing Unit (machines with serial number 50,000 and above) in the IBM System/360 Model 20. Volume 2 contains operations information (Section 5) and Volume 1 contains information on the following:

Diagnostic techniques (Section 1)
Error conditions (Section 2)
Data flow (Section 3)
Functional units (Section 4)
Power (Section 6)
Microprograms (Appendix B)

Both volumes are used for maintenance, instruction, and recall.

The material in these volumes supplements the information contained in the following manuals:

1. Field Engineering Theory of Operation, *2020 Processing Unit, System/360 Model 20 (Machines with serial no. 50,000 and above),* Form Y33-1021.
2. Field Engineering Maintenance Manual, *2020 Processing Unit, System/360 Model 20 (Machines with serial no. 50,000 and above),* Form Y33-1035.

Associated Publications

The following Field Engineering Maintenance Diagrams manuals contain information on the features which may be installed on the 2020 Processing Unit:

1. *1403 Printer Models 2, 7, N1 Attachment Feature, System/360 Model 20 (Machines with serial no. 50,000 and above),* Form Y33-1018.
2. *2152 Printer-Keyboard Attachment Feature, System/360 Model 20 (Machines with serial no. 50,000 and above),* Form Y33-1026.
3. *2203 Printer Attachment Feature, System/360 Model 20 (Machines with serial no. 50,000 and above),* Form Y33-1022.
4. *2520 Card Read Punch Attachment Feature, System/360 Model 20 (Machines with serial no. 50,000 and above),* Form Y33-1028.
5. *2560 Multi-Function Card Machine Attachment Feature, 2501 Card Reader Attachment Feature, 1442 Card Punch Model 5 Attachment Feature, System/360 Model 20 (Machines with serial no. 50,000 and above),* Form Y33-1033.
6. *Binary Synchronous Communications Adapter, System/360 Model 20 (Machines with serial no. 50,000 and above),* Form Y33-1039.
7. *Input/Output Channel Feature, System/360 Model 20 (Machines with serial no. 50,000 and above),* Form Y33-1017.
8. *Storage Control Feature, System/360 Model 20 (Machines with serial no. 50,000 and above),* Form Y33-1037.

Information on the serial I/O channel feature is contained in Field Engineering Theory of Operation, Maintenance Diagrams, *Serial I/O Channel Attachment Feature, System/360 Model 20 (Machines with serial no. 50,000 and above),* Form Y33-1040.

The associated Field Engineering Theory of Operations manual for the features are:

1. *1403 Printer Models 2, 7, N1 Attachment Feature, System/360 Model 20 (Machines with serial no. 50,000 and above),* Form Y33-1020.
2. *2152 Printer-Keyboard Attachment Feature, System/360 Model 20 (Machines with serial no. 50,000 and above),* Form Y33-1025.
3. *2203 Printer Attachment Feature, System/360 Model 20 (Machines with serial no. 50,000 and above),* Form Y33-1027.
4. *2520 Card Read Punch Attachment Feature, System/360 Model 20 (Machines with serial no. 50,000 and above),* Form Y33-1029.
5. *2560 Multi-Function Card Machine Attachment Feature, 2501 Card Reader Attachment Feature, 1442 Card Punch Model 5 Attachment Feature, System/360 Model 20 (Machines with serial no. 50,000 and above),* Form Y33-1034.
6. *Binary Synchronous Communications Adapter, System/360 Model 20 (Machines with serial no. 50,000 and above),* Form Y33-1038.
7. *Input/Output Channel Feature, System/360 Model 20 (Machines with serial no. 50,000 and above),* Form Y33-1019.
8. *Storage Control Feature, System/360 Model 20 (Machines with serial no. 50,000 and above),* Form Y33-1036.

Second Edition (November 1969)

This volume is a major revision of, and obsoletes, Y33-1042-0.

Changed diagrams are denoted by the symbol ● to the left of the caption, small changes being also indicated by vertical lines to the left of the changes.

Changes are continually made to the specifications herein; any such changes will be reported in subsequent revisions or FE Supplements.

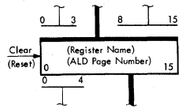
A form for readers' comments is provided at the back of this publication. If the form has been removed, comments may be addressed to IBM Laboratories, Product Publications, Dept 784, 703 Boeblingen/Wuertt, P.O. Box 210, Germany.

Contents

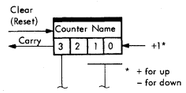
Note: The diagrams in this manual have a code number to the right of the caption. This is a publishing control number and is unrelated to the subject matter.

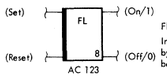
Legend

1. Logic Diagrams

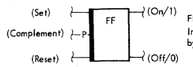


Register, Counter
Input side is denoted by thick line. A partial transfer of contents is shown by numbered input and/or output lines.

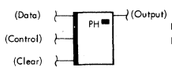




Flip Latch
Input side is denoted by thick line. Circuit multiples shown by numeral in lower right corner. ALD reference page may be shown beneath.



Flip-Flop
Input side is denoted by thick line. Shift signal is shown by a P or N.



Polarity Hold
Input side is denoted by thick line.

AND

OR

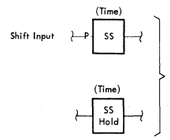
Exclusive OR

Negator (Inverter)

Negative Polarity wedge

Adder

Gate
Numerals against gate symbol give page or diagram number of gating circuit.

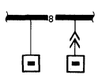


Singleshot

Oscillator

Time Delay

Indicator lamp



Identifies indicatable bus, register, latch, ect. such as: Indicatable bus with number of bus lines indicated

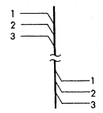
Indicatable flip latch

Parity Check data bus

Parity Generate data bus

Amplifier
XX Abbreviations:
CD = Core Driver
HD = Head Driver
ID = Indicator Driver
LD = Line Driver
LT = Line Terminator
MD = Magnet Driver
V = Voltage Amplifier

Interface
Denotes interface between two units.

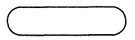


Multiple Line Transfer

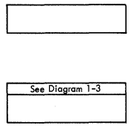
2. Timing Charts

Active State
Numerals at beginning and end of the bar identify the signal(s)(also on the same chart) that activate and deactivate this line "Not" with the number indicates that lack of the signal conditions the line.

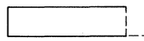
3. Flowcharts



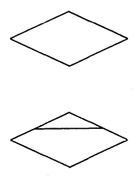
Terminal
Indicates beginning or end of event



Process
Indicates a major function or event. The upper portion of a divided block specifies where a detailed flowchart of the process is located.

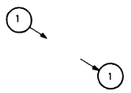


Annotation
Gives descriptive comment or explanatory note.



Decision
Indicates a point in a flowchart where a branch to alternate paths is possible. The upper portion of a divided block specifies where a detailed flowchart is located.

4. General

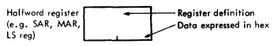


On-Page Connector
Indicates connection between two parts of the same diagram. Arrow leaving symbol points (line-of-sight) to correspondingly-numbered symbol.

On-Page Connector
Indicates connection between two parts of the same diagram. Alphameric grid coordinate of complementary connector shown beneath.

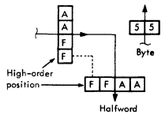
Off-Page Connector
Indicates connection between diagrams located on separate pages. Location of correspondingly-lettered symbol shown adjacent.

5. Special Symbols



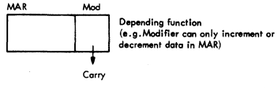

Decision by circuits


Exchange of bytes (cross shift)

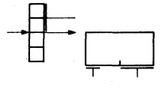


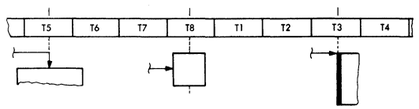
Information blocks showing which data (hex) is on a line, and an input or output of a functional unit


Subfunction, e.g. Address checking (AC)

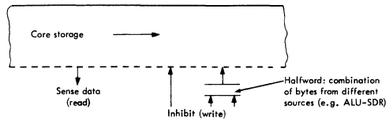


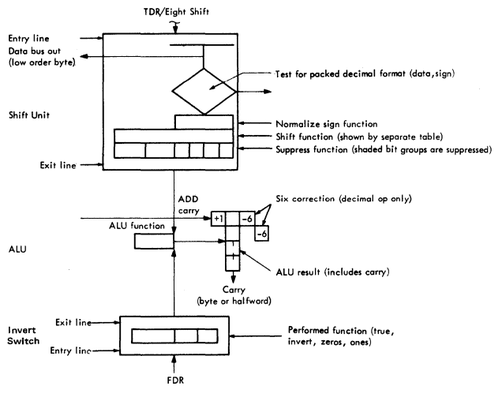
Depending function (e.g. Modifier can only increment or decrement data in MAR)


Partial use of data (byte, half byte, or bit)



Alignment of functional blocks with basic timing





Logical unit comprising shift unit, ALU, and invert switch. Functions not used within a specified operation are deleted. The whole logical unit is controlled by signals timed by cycles (eg. FDR true 0-15 during cycle 1). For charts representing more than one different operation, the different functions are repeated and identified by mnemonics

6. Standard Signal Arrangement

Signal grouping according to functional units	No	Name	ALD
LS zone selection	1	Sense Trap Request Lines	LA103
	2	LS New PL Zone Gate	KA511
	3	LS Current PL Zone Gate	
	4	New/Current PL	
	5	CE LS Select	CC222
Spare	6		
LS register selection, LS input and output control	7	Fixed X-Address	LA412
	8	'To Reg' Select	LA402
	9	'From Reg' Select	LA411
	10	LS to SAR	KB411
	11	LS to MAR	
	12	LS to FDR	KB401
	13	LS to TDR	
	14	MAR to LS	LA702-712
	15	Set ALU (I/O Bus) to LS	
	16	LS Write	LA302/313
Spare	17		
MAR/modifier control	18	Set Address Check	RA501
	19	Branch Go	RA502
	20	Increment by 1	RA402
	21	Increment by 2	RA403
	22	Decrement by 1	RA401
	23	Decrement by 2	RA402
	24	Prevent Mod-SAR-Inh Check	KA511
Spare	25		
SDR control	26	Prevent Storage Use	MA402
	27	SDR to Inh	MA401
	28	SDR to Op Reg	KB102
Spare	29		
TDR/shift unit control	30	SDR to TDR	KB402
	31	Eight Shift Control	RB162
	32	Shift by 2 or 4	RB161
	33	No Shift	RB162
	34	Test Packed Byte or Sign	RA502
	35	Normalize Sign Active	
	36	Suppress	RB171
Spare	37		
FDR/invert switch control	38	ALU to FDR	AA303
	39	Reset FDR/Retain FDR 0-7	AA303/KB411
	40	Invert Switch Control	RB301
Spare	41		
ALU control	42	ALU Control Gate	AA301
	43	Additional Carry	AA302
	44	Six Correction 8-11/12-15	
	45	Set Carry Latch	AA402
	46	Set Condition Code Latches	
	47	ALU to Inh	MA401
	48	ALU to SAR	KB411
Spare	49		
I/O bus control	50	Data Switch to Op Reg	KB402
	51	Op Reg to Address Bus	KA541
	52	I/O Display Address Out	
	53	Allow Strobe	
	54	SENS Strobe/Control Strobe	BA102
	55	Sense Reset/CTRL Strobe	
	56	Prevent ALU and SU Check	BA103
	57	I/O Bus to FDR	
Spare	58		
	59		
	60		
	61		
	62		
	63		
	64		
	65		
	66		
Set CPU checks	67	Set ALU Test Latch	CC121
	68	Set Process Check	CC122
	69	Set LSA Check	CC221
	70	Set Mod Check	CC101
	71	Set SU Check	CC102
	72	Set ALU Check	
	73	Set Bus Check	
	74	Set SAR Check	CC101
	75	Set Inh Check	

Combined signal which shows when new and current PL may differ (higher priority trap request). Depending upon the zone gates, the last instruction is finished in the currently selected LS zone while the next instruction is already initiated using the new LS zone.

Combined signal. The number above the signal shows which LS register is addressed.

Combined signal comprising: TDR 0-7 to SU 0-7, TDR 8-15 to SU 8-15 } No shift B; TDR 0-7 to SU 8-15, TDR 8-15 to SU 0-7 } Cross shift

Combined signal comprising: Shift left by 2, Shift left by 4, Shift right by 2, Shift right by 4

Combined signal comprising: No shift 0-7, No shift bit 8-15 } No shift 0-15

Combined signal comprising: Suppr SU bit 0-7, Suppr SU bit 0-3, Suppr SU bit 4-7, Suppr SU bit 8-11, Suppr SU bit 12-15, Suppr SU bit 8-9, Suppr SU bit 10-11, Suppr SU bit 12-13, Suppr SU bit 14-15

Combined signal comprising: FDR true 0-15, FDR invert 8-15, FDR invert 0-7. FDR invert 0-7 is forced by FDR invert 8-15. If FDR invert 0-7 is not required, it is suppressed. True = true; Invert = invert; Invert and true = force zeros; Not invert not true = force ones

Combined signal comprising: Adder gate, AND gate, OR gate, OE = no gate active

Signals prefixed by "Set" are internal card signals which cannot be measured. They indicate when the specified function is executed.

Reference to a single ALD page or to the first of a group of pages.

Abbreviations

AC	Address Check
ADDR, Addr, ADR	Address
ALC	Auto Length Count
ALU	Arithmetic and Logic Unit
ASCII	American Standard Code for Information Interchange
Aux	Auxiliary
BSCA	Binary Synchronous Communications Adapter
CC	Condition Code
CE	Customer Engineer
Chk, Ck	Check
CLD	Control Logic Diagram (microprogram list)
Col Bin	Column Binary
CPL	Control Program Load
CPU	Central Processing Unit
CS	Cycle Steal
Cust	Customer
CY	Cycle
Diag	Diagnostic, Diagram
Displ, Dply	Display
DR	Data Register (display customer console)
EBCDIC	Extended Binary-Coded-Decimal Interchange Code
Ex	Execution
FDR	From-Data Register
FL	Flip Latch (Latch)
IAR	(Micro) Instruction Address Register
ICPL	Initial Control Program Load
ICR	Impulse Check Routine
Indir	Indirect
Inh	Inhibit (switch)
Insn, Instr	Instruction
IOC	Input/Output Channel
I/O	Input/Output (Device)
I-Recall Addr	Instruction-Recall Address
LC	Length Count
LS	Local Store
MANOP	(Circuit-Controlled) Manual Operation
MAR	Modify Address-Register
MFT	Machine Function Test
Mnem	Mnemonic
NSI	Next Sequential Instruction
OE	Exclusive OR
Op	Operation
Op Reg	Operation Register
Oprnd	Operand
PL	Program Level
Pri	Primary
PSW	Program Status Word
Rd	Read
Reg	Register
Req	Request
Rst	Reset
SAR	Storage Address Register
SC	Set Carry
SDR	Storage Data Register
Stor	Storage
SU	Shift Unit
Sw	Switch
Syst	System
T	Time (pulse)
TDR	To-Data Register
u-instr	Microinstruction
Wkg	Working
△CY	Delta Cycle
/..../	Representation of Hexadecimal Numbers

WHAT CAN THE CPU DO?

Circuit-controlled operations

Microinstruction-controlled operations

Documented by microprogram lists (CLD's) and by flowcharts. The CLD's are available in binders C01 to C03. Flowcharts are given in 2020 FEMDM, Volume 1, Appendix B. Flowcharts for special E-phases of I/O instructions (XIO, TIO, TIOB, CIO), special parts of service phases, and special routines (I/O log in, CE) are given in the corresponding "Attachment"-FEMDM. Maintenance programs are documented in binders labeled T10, T30, and T40.

Mode Switch (customer console)

PROCESS

INSN STEP
STOR DPLY
STOR ALTER
STOR SCAN

ADR STOP
DPLY REG
ALTER REG
STOR FILL

CPL

Usemeter key to CE and CE mode switch on — No / Yes

Execution of 43 basic microinstructions

Depending upon direct or indirect operand addressing, 113 varieties of the 43 basic microinstructions are possible

Additionally, 18 of the microinstr's can operate in auto-length-count mode (ALC)

(Documented by Diagrams 5-3 to 5-72)

(Documented by Diagram 5-81)

CPU cycle steal operation

CPU cycle steal (CS) operations can be requested by the storage control feature, IOC, and BSCA (CS requests). Consider the operations as circuit controlled service phases which allow rapid data transfer from or to CPU. CS operations are of highest priority

MANOP's

Storage Display
Storage Scan
Storage Alter
Storage Fill
Storage Test
Local Store Display
Local Store Alter
Initial Control Program Load (ICPL)
CPU LOG IN

CE storage test switch on

(after CPU LOG IN) — Yes

Usemeter key to CE and CE mode switch on — No

Initially performed if: 1. Power on, or
2. System reset key, or
3. Load key operated (ICPL, CPL, customer program load).

(Documented by Diagrams 5-73 to 5-80)

The microinstructions are linked to the micro-control-program.
The whole micro-control-program consists of routines. The routines are designed to execute following main CPU functions:

1. Control Program Load (CPL). Microinstruction-controlled loading of the micro-control-program after the first loader card has been read into core storage by MANOP ICPL. In customer mode, CPL is performed using the core resident absolute loader in core storage (Aux storage)
2. System Reset Routine
3. Manual Routines. Micro-control-program to display or alter the 8 general registers (customer), PSW, I-recall address, and machine language instruction op code, or to perform instruction step, and address stop
4. Load Routine. Micro-control-program which simulates an XIO machine language instruction to read the first loader card of the customer program
5. Instruction Phase (I-Phase) and Execute Phase (E-Phase) of the Machine Language Instructions
6. I/O Service Phases
7. Interrupt Handling
8. Program Error Handling
9. Maintenance. I/O log in routines (detailed and count type log)

CPU micro test, CPU loader test. Worst case pattern test (core storage adjustments)

Machine function tests (MFT's) and impulse check routine (ICR). Both tests run on a mixture of special micro-control-program routines and machine language instructions

● Diagram 5-1. CPU Operations (Part 1 of 2) (03705A) 2020 ≥50,000 FEMDM Vol 2 (8/69)

Microinstruction Layout

Halfword: High-order Byte (0 1 2 3 4 5 6 7) | Low-order Byte (8 9 10 11 12 13 14 15)

RI Format

	Mnemonic	0 1 2 3	4	5 6 7	8 9 10 11 12 13 14 15	Condition Code Setting	Updating Operand-Addresses	Auto Length Count (ALC)	Remarks	Diagram Number (5 - ...)
Immediate Byte Instructions: Load Byte Immediate	LBI	/0/	0	To Reg	Immediate Data Byte					3 (e.g. 5-3)
Insert Byte Left	IBL		1							4
AND Immediate	ANDI	/1/	0							5
OR Immediate	ORI		1							
Exclusive OR Immediate	EORI	/2/	0							6
ADD Immediate	ADDI		1							7
Test Under Mask and Skip if Zero	TMSZ	/3/	0							
Test Under Mask and Skip if Not Zero	TMS		1							
Translate and Branch Short	TRBS	/4/	0						TRBS, TRBL: Indirect address if bit 15 of branch address is on	8 9
Translate and Branch Long	TRBL		1							10 11

Direct / Indirect

RD Format

	Mnemonic	0 1 2 3	4	5 6 7	8 9 10 11 12 13 14 15	Diagram Number
Load/Store: Load Halfword	LH	/5/	0	To Reg	Displacement Address	12 13
Store Halfword	STH		1			14 15
Branch Type Instructions: Branch and Store	BST		1	1 1 1 1		16 17
Branch on Binary Zero	BZ	/6/	0	To Reg		18 19
Branch on Binary Minus	BM		1			
Branch on Binary Plus	BP	/7/	0			20 21
Branch on Address Check	BAC		1			
Branch Unconditional	B	/8/	0	0 0 0		

Direct addressing if 0
Indirect addressing if 1

FF instruction bits 8 12
0 0 = DD
0 1 = DX
1 0 = XD
1 1 = XX

Instruction Type: DD DX XD XX (ALC)

FF Format

	Mnemonic	0 1 2 3	4	5 6 7	8 9 10 11 12 13 14 15	Condition Code Setting	Updating Operand-Addresses	Auto Length Count (ALC)	Diagram Number
Move Type Instructions: Store Zone Register	STR	/8/	0	0 0 1 0 0	0				22
Load Zone Register	LR		0	0 0 1 1 0	0				23
Move Halfword and Split	MVHS		1	Split AC 0			+2		24 25
Shift Left and Move	SLM	/9/	0	Shift Amount					26 27 28 29
Shift Right and Move	SRM		1				+/- 2		30 31 32 33
Move Halfword	MVH	/A/	0	1 Addr +or-	(+ if 1, - if 0)		+/- 1		34 35 36 37
Move Byte	MVB		1	0			+1		38 39 40 41
Move Numeric	MVN		1	1 0					
Move Zone	MVZ		1	1 1					
Binary Arithmetic Instructions: Add Halfword	AH	/B/	0	0	To Reg	From Reg	-2	ALC: If XX-type instruction and 'to reg'=3, 'from reg'=5	42 43 44 45
Add Halfword and Set Carry	AHSC		0	1					
Subtract Halfword	SH		1	0					
Subtract Halfword and Set Carry	SHSC		1	1					
Logical Instructions: AND Byte or Halfword	AND	/C/	0	0	Address Check (AC) / Condition Code		+1		46 47 48 49
OR Byte or Halfword	OR		0	1					
Exclusive OR Byte or Halfword	EOR		1	0					
Compare Logical Byte or Halfword	CLC		1	1					
Packed Decimal Instructions: Add Packed Byte	AP	/D/	0	0 0					50 51 52 53
Subtract Packed Byte	SP		0	0 1					54 55 56 57
Zero and Add Packed Byte	ZAP		0	1 0					58 59 60 61
Perform Packed Complement	PPC		0	1 1					54 55 56 57
Set Decimal Sign	SDS		1	0 0					58 59 60 61
CPU Stop Instruction: Halt and Display Halfword	HALT		1	1 0 0	0		Unconditional: -1		62 63 64 65
					0				66

Conditional (instruction bit 6 on)

Operand addressing:
if bits 0 = direct
if bits 1 = indirect

Direct Indirect ALC

I/O Instructions

	Mnemonic	0 1 2 3	4	5 6 7	8 9 10 11 12 13 14 15	Updating Operand-Addresses	Auto Length Count (ALC)	Diagram Number
Sense I/O	SENS	/E/		To Reg	SENS/CTRL Address	+1	ALC if indir address and 'to reg' = 7	67 68 69
Control I/O	CTRL	/F/						70 71 72

ADDRESS CHECK (AC, bit 7 of FF format instructions).
When the bit is on, the operand addresses (in 'to' or 'from reg' if indirect address) are checked that they are not outside customer storage area. For halfword instructions (e.g. MVHS, MVH, AH), the addresses are also checked for halfword boundary (address must be even). An address check stops the CPU by program check (trap request 2).

SPLIT (bits 5 and 6 of MVHS).
During MVHS, a halfword is split. The result of the split is set into two adjacent registers. The binary value of bits 5 and 6 (0-3) defines the split mode. Details of split are given in the MVHS flowchart.

SHIFT AMOUNT (bits 5, 6, and 7 of SLM, SRM).
The pattern in these bits specifies the number of bits by which the operand halfword has to be shifted.

Bits 5 6 7	
0 0 0	Shift by 0 (No shift, only move)
0 0 1	Shift by 2
0 1 0	Shift by 4 No shift by 6 (bits 6 and 7 on simultaneously)
1 0 0	Shift by 8
1 0 1	Shift by 10
1 1 0	Shift by 12

'TO REG', 'FROM REG'.
These fields may contain any binary value from 0 to 7. This binary value is used to select one of eight local storage registers in a local store zone. For FF and I/O instructions, the selected register is used as data register if the high-order bit in the 'to or from reg' field is off (direct addressing). The selected register is used as address register for a core storage operand if the high-order bit is on (indirect addressing).
When the 'to reg' specifies local store register 7 (IAR, instruction address register), instructions which set data into a local store register as a result of their operation (load type instruction) are treated as no operation.

Example of Microprogram List (CLD)

Heading

```
ADDR  INST   TO    LABEL  MNEM OPERANDS      STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX    COMMENTS
                         -FROM- JK62
JK74 6184  JKR4           BZ   1,DIGSFL      BR TO IAR.0-7/INST.8-14 IF R1 = 0
JK76 29FE                 ADDI 1,-2          R1 *= R1 + 'FFFE'
JK78 7164  JK64           BP   1,START       BR TO IAR.0-7/INST.8-14 IF R1 ,GT, 0
JK7A 6990  JK80           BM   1,SIGNST      BR TO IAR.0-7/INST.8-14 IF R1 ,LT, 0
           *   FIELD SEPARATION CHARACTER
JK7C 8A66                 SH   6,6,CC        CC, R6 *= R6 - R6
JK7E 8066  JK66           B    FILL          BR TO IAR.0-7/INST.8-14
           *   SIGNI ICANCE START CHARACTER
JK80 7684  JKR4  SIGNST BP   6,DIGSFL       BR TO IAR.0-7/INST.8-14 IF R6 ,GT, 0
                         -FROM- JK7A
JK82 C461                 OR   6,1           R6 *= R6 ,OR,R1
JK84 68AA  JKAA  DIGSFL BM   0,SCNDGT       BR TO IAR.0-7/INST.8-14 IF R0 ,LT, 0
                         -FROM- JK74  JK80
JK86 ABOD                 MVR  0,5I,INC,AC   R0 *= R0.0-7/BY(R5, AC, +1)
JK88 8A00                 MVHS 0,0,1         R0 *= '0000'/R0.12-15 , R1 *= '01'/R0.0-11
```

Branch To

End Line

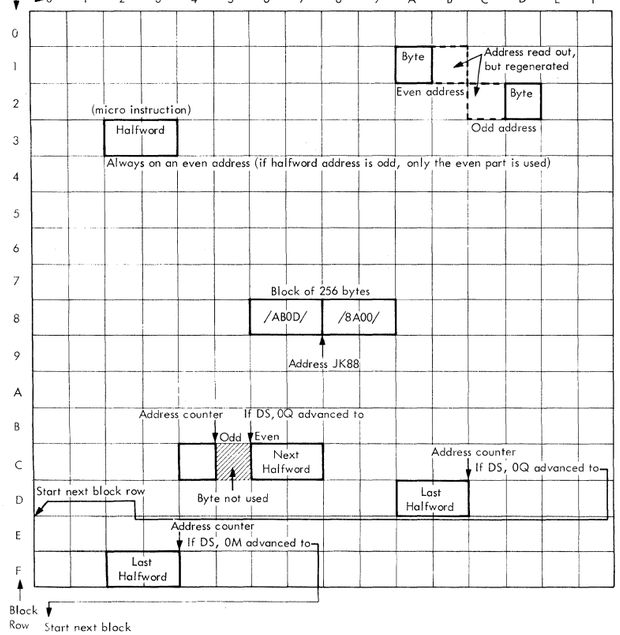
```
0JHA  CPU2 BASIC ROUTINES          LSTPN4682503  FC012810 30SEP68 0CKPN4682502  FC012810      PAGE  16
```

eg. JK 8 8

Symbolic Block Address

Block Addr

Hex Contents of the Addressed Halfword



The real values of the symbolic block addresses depend upon system configuration and main-storage size.
The references of symbolic and real block addresses are given in the LINK LIST which can only be printed immediately following the loading of the microprogram.

Common Symbols
'To reg' = 0-7.
'From reg' = 0-7.
I = the corresponding reg or label is used for indirect addressing.
AC = address check performed.
INC = the indirect address (in reg) is incremented.
DEC = the indirect address (in reg) is decremented.
CC = condition code set.
NC = no condition code.
X'a...' = any hex digit 0 to F.
[ ] = optional function.

Label Required Allowed

Microinstructions

X		LBI IBL ANDI ORI EORI ADDI TMSZ TMS	'To reg', X 'aa' or 'To reg', n or 'To reg', -n
X		TRBS	'To reg', label [X 'a']
X		TRBL	'To reg', B (label)
X		LH STH BZ BM BP BAC	To reg, label [±n][, I]
X		BST B	Label [±n][, I]
X		LR STR HALT	'To reg', 'from reg'
X		SLM SRM	'To reg'[I], 'from reg' [I], n
X		MVHS	'To reg', 'from reg' [I] , n, [AC]
X		MVH	'To reg'[I] 'from reg'[I], INC[,AC]
X		MVB	or 'To reg' [I],'from reg' [I], DEC [,AC]
X		MVN MVZ AP ZAP SP PPC SDS	'To reg' [I], 'from reg' [I] [,AC]
X		AH AHSC SH SHSC AND OR EOR CLC	'To reg' [I], 'from reg' [I], CC[,AC] or 'To reg' [I], 'from reg' [I], NC[,AC]
X		SENS	'To reg' [I], X'aa' or
X		CTRL	'To reg' [I], label [±n]
X		DC	A (label [±n])
X		DC	E (label, label)
X		DC	B (label)
X		DC	D (Label [±n])
X		DC	C 'ABCDEFGH.....'
X		DC	X 'aaaa.....'
		ORG	* ±n
		ORG	Label
	X	START	X 'aaaa'
		ENTRY	Label
		EXTRN	Label
X		DS	n
X		DS	0H
X		DS	0Q
X		DS	0M
	X	EQU	X 'aaaa'
	X	EQU	Label [±n] or*
		END	Label

Assembler Instructions

n = 0 through 127
-n = -1 through -128

n = 0 through 255, however, the result of label ±n must be an address inside block boundary

n = 0,2,4,8,10,12 (Shift amount)

n = 0 to 3 (Split mode)

n = 0 through 255, however, the result of label ±n must be an address inside block boundary

END. The assembler branches to the address defined by the label (start microprogram) and executes microinstructions.

DEFINE CONSTANT. The constants are hexadecimal digits (up to 16), characters (up to 32) or addresses. The addresses are of four different types (A, E, B, D).

- Type A = halfword address defined by label or by label ± n (n = 0 to 255).
- Type E = an internal label is similar to an external label. The constant is the address defined by the external label.
- Type B = the constant is the block address (high-order byte) of the address defined by the label.
- Type D = the constant is the low-order byte of the address defined by the label or by the label ± n (n = 0 to 255).

ORIGIN. Command for the address counter of the assembler to go either to the ORG address ±n (if ,n = 0 to 255) or to the address specified by the label.

START. The start address of a section is defined. The required label is used as section name.

ENTRY/EXTERN. The label defines an address at which the section is entered from another section (ENTRY) or to which the program goes on leaving the section.

DEFINE STORAGE. Command for the assembler to advance the address counter.
The counter is advanced either according to n (N = 0 to 255) or to a storage boundary defined by 0H, 0Q, or 0M:

- 0H = continue at next halfword address.
- 0Q = continue at start address of next block row.
- 0M = continue at start address of next block.

(see examples in the block on the left)

EQUATE. The required label is equated either with the direct address (X'aaaa'), with the address defined by the label, or with the address defined by the label ±n (n = 0 to 255).
For EQU* the required label is equated with the address presently in the address counter.

The statement is represented by a formula which defines the detailed CPU functions required to perform a microinstruction. The detailed CPU functions are also outlined in the operation flowcharts.

EXAMPLE

```
AP    4I,2I,AC    CC,C/BY(R4,AC)←BY(R4,-1),D+,BY(R2,AC,-1),D+,C
```

Result *= Operation

Consider as an arrow

Direction of Reading

The result of the operation (see "Summary") is set into the byte (BY) addressed by LS reg 4 (R4, AC). The address is checked. A carry, when decimal adding the operands, is saved by setting the carry latch (C/). The condition code (CC) latches are set.

*=

1. Define operands: BY, D+, BY, D+, C (Two bytes and a previous carry are decimal added.)
2. Define addressing: BY (R4), BY (R2) (One byte is addressed by LS reg 4, the other by LS reg 2.)
3. What happens with the addresses? (R4, -1), (R2, AC, -1) (Both addresses are decremented by 1. The address in LS reg 2 is checked.)

Summary
The byte addressed by LS reg 2 and a present previous carry are decimal added to the byte addressed by LS reg 4. The addresses are decremented by 1 and checked.
NOTE: AC specification is valid for all indirect addresses in an instruction.

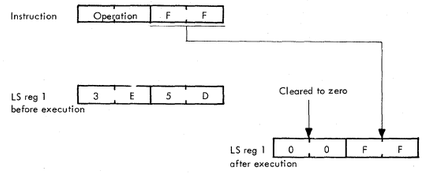
Statement Symbols

A	= Logical and	PIUL	= Customer Console Display
AC	= Address Check	PL	= Program Level
BR	= Branch	R	= Local Storage Register
BY	= Byte	SKIP	= Skip Over the Next Instruction
C	= Carry	SL	= Shift Left
CC	= Condition Code	SR	= Shift Right
COMP	= Compare	TDR	= Dataflow Register
D+	= Decimal Plus	UNTIL	= Length'n-count Reduction Until.....
D-	= Decimal Minus	VALID SIGN	= Decimal Sign
ESTR	= Customer Console Display		Hex A to F
FDR	= Dataflow Register	+	= Binary Add
GT	= Greater Than	-	= Binary Complement Add
HW	= Halfword	.	= Precedes a Bit Notation
IAR	= Microprogram IAR	,	= Separator
INDIR	= Indirect	/	= Connection of Values
INST	= Instruction	( )	= Contains an Address
INVALID	= Invalid Address	8-15	= Bits 8-15 (Example)
LT	= Less Than	X	= Secondary Defined Value
NE	= Not Equal	*=	= Direction of Data Transfer (⟸)
NORMALIZED	= Decimal Sign For EBCDIC or USASCII	'XXXX'	= Hexadecimal Representation
NOT C	= Logical "1" if No Carry		
OE	= Exclusive OR		
OR	= Logical OR		

Alphabetic Listing of Microinstructions

Mnemonic	Diagram
ADDI	5-6
AH	5-42,43,44,45
AHSC	5-42,43,44,45
AND	5-46,47,48,49
ANDI	5-5
AP	5-54,55,56,57
B	5-20,21
BAC	5-18,19
BM	5-18,19
BP	5-18,19
BST	5-16,17
BZ	5-18,19
CLC	5-50,51,52,53
CTRL	5-70,71,72
EOR	5-46,47,48,49
EORI	5-5
HALT	5-66
IBL	5-4
LBI	5-3
LH	5-12,13
LR	5-23
MVB	5-34,35,36,37
MVH	5-30,31,32,33
MVHS	5-24,25
MVN	5-38,39,40,41
MVZ	5-38,39,40,41
OR	5-46,47,48,49
ORI	5-5
PPC	5-58,59,60,61
SDS	5-62,63,64,65
SENS	5-67,68,69
SH	5-42,43,44,45
SHSC	5-42,43,44,45
SLM	5-26,27,28,29
SP	5-58,59,60,61
SRM	5-26,27,28,29
STH	5-14,15
STR	5-22
TMS	5-7
TMSZ	5-7
TRBL	5-10,11
TRBS	5-8,9
ZAP	5-54,55,56,57

The immediate data byte is loaded into the low-order byte of the LS register specified in the 'to reg' field of the instruction. The high-order byte is set to zero.



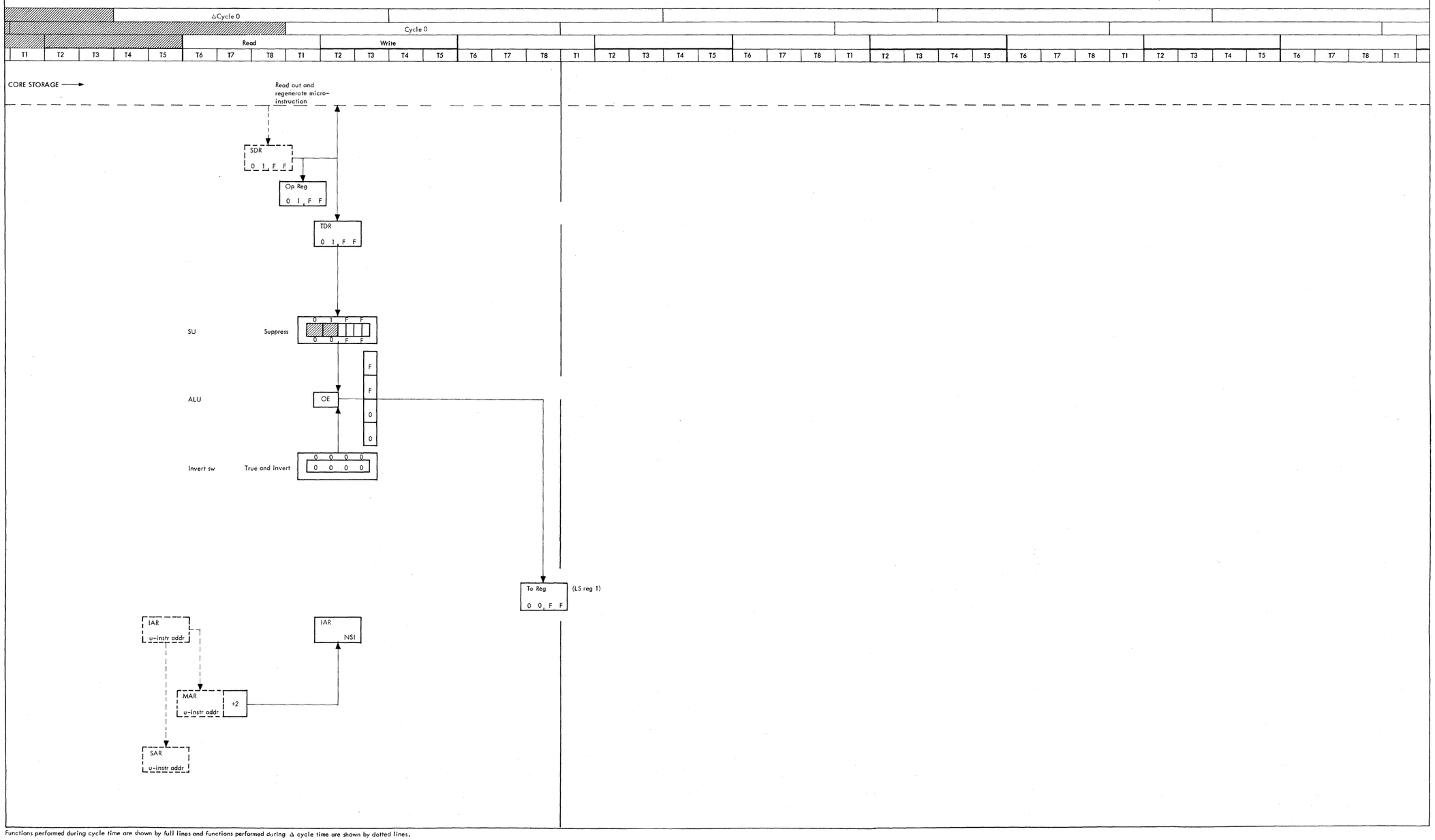
Microinstruction Layout

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Op Code					To Reg			Immediate Data							
0				0											

Mnemonic
LBI
Format
RI
Type

INST MNEM OPERANDS STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX

01FF LBI 1,X'FF' R1+='00FF'

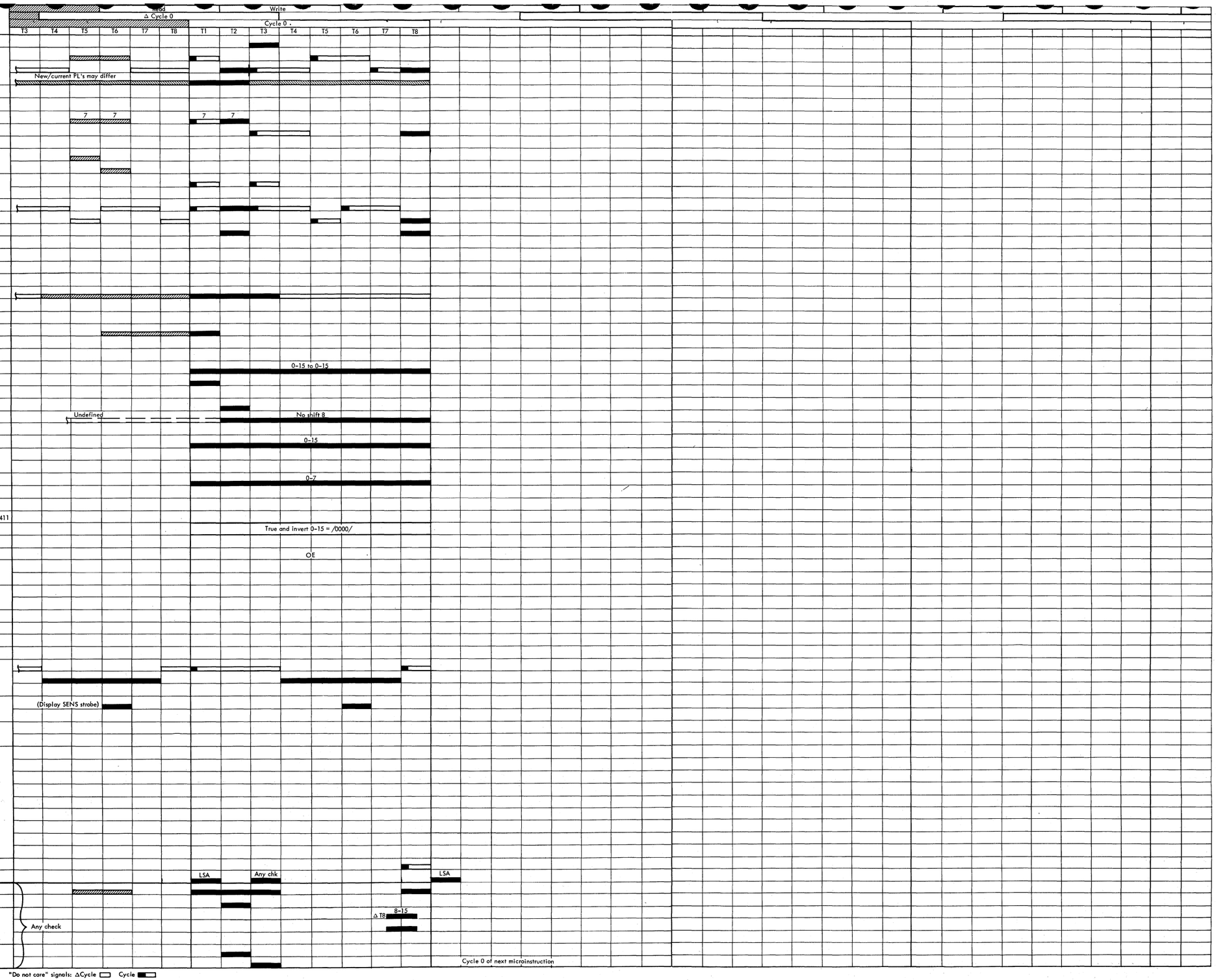


Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
△Cycle
Cycle

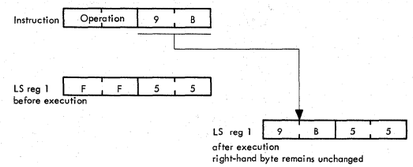
Functions performed during cycle time are shown by full lines and functions performed during △ cycle time are shown by dotted lines.

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702
15	ALU (I/O Bus) to LS	KB412
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Modifier Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59		
60		
61		
62		
63		
64		
65		
66		
67	Set ALU Zero Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▭

The immediate data byte is loaded into the high-order byte of the LS register specified in the 'to reg' field of the instruction. The low-order byte remains unchanged.

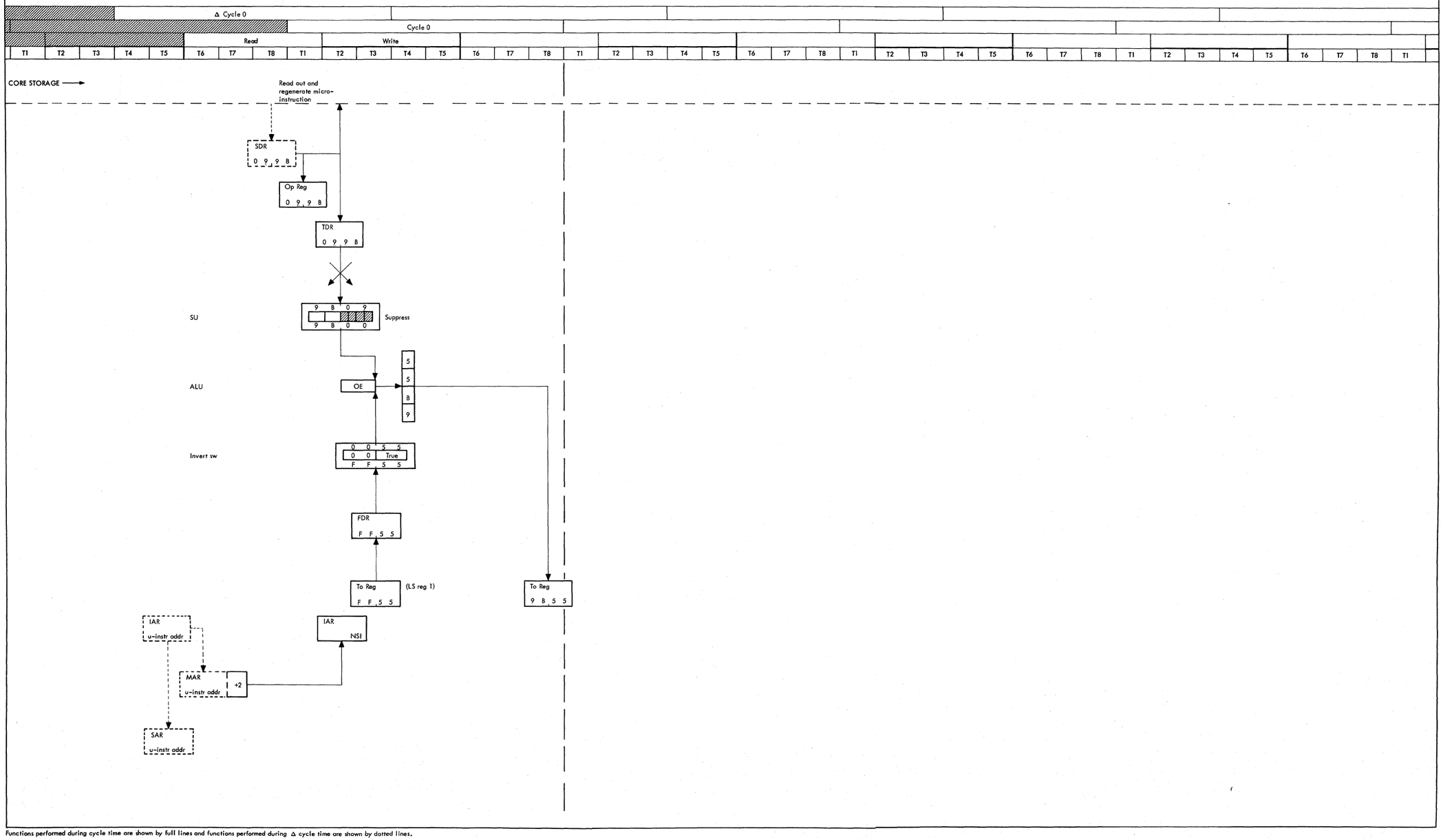


Microinstruction Layout

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Op Code					To Reg			Immediate Data							
0				1											

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
099B	IBL	1,X'9B'	R1⇐'9B'/R1.8-15

Mnemonic
IBL
Format
RI
Type

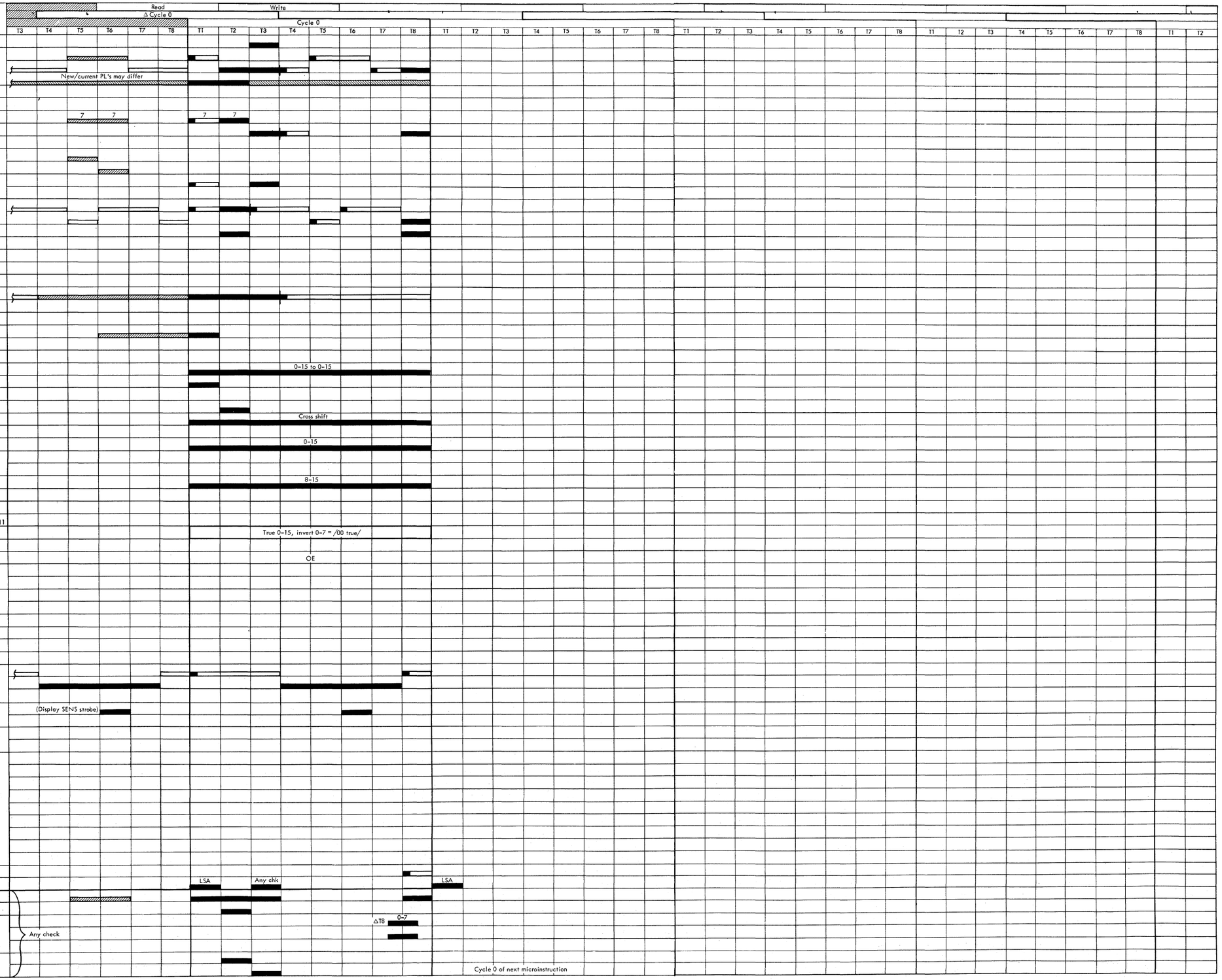


Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle

Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59		
60		
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	

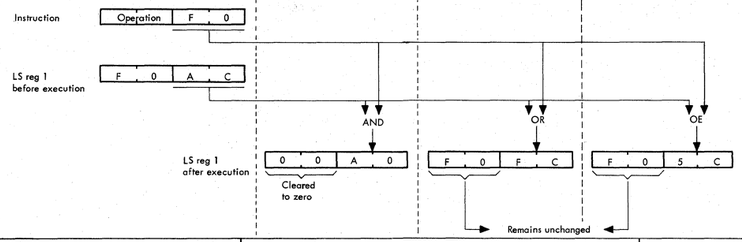


Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▬

● Diagram 5-4. Insert Byte Left (Part 2 of 2) (03709A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

The immediate data byte is ANDed, ORed, or exclusive ORed with the low-order byte in the 'to reg'. The result is set into the 'to reg'.

For ANDI the high-order byte is set to zero. The high-order byte remains unchanged for ORI and EORI.

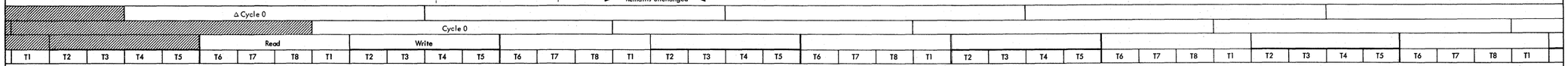


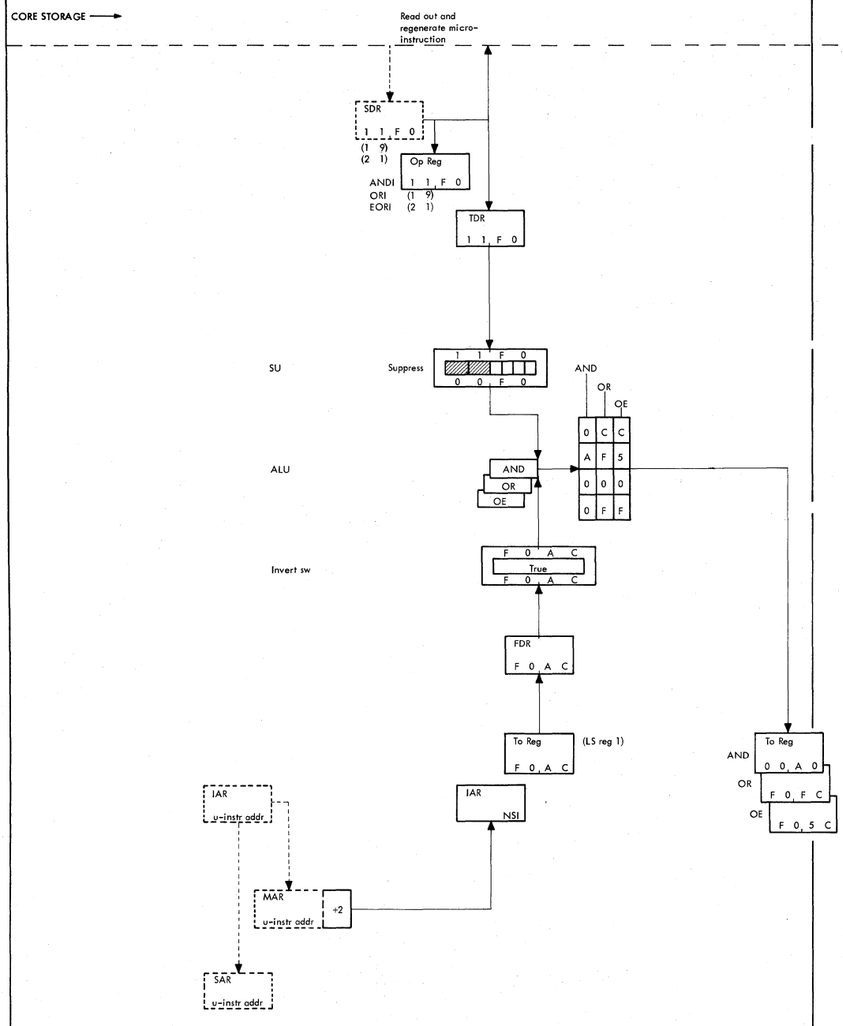
Microinstruction Layout

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
Op Code					To Reg			Immediate Data								
1				0												ANDI
1				1												ORI
2				0												EORI

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
11F0	ANDI	1,X'F0'	R1+=R1,A,'00F0'
19F0	ORI	1,X'F0'	R1+=R1,OR,'00F0'
21F0	EORI	1,X'F0'	R1+=R1,OR,'00F0'

Mnemonic
ANDI
ORI
EORI
Format
RI
Type





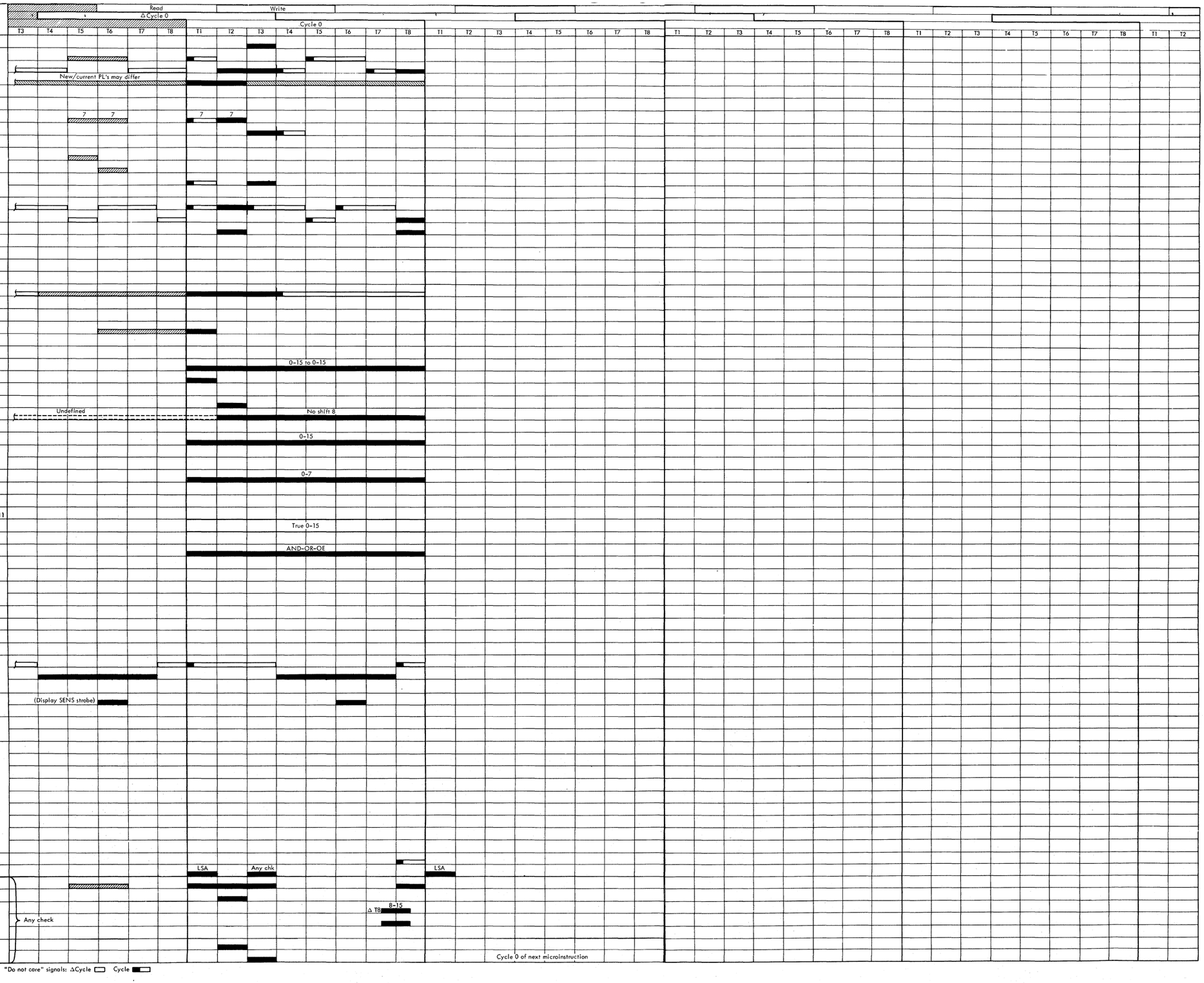
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle

Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

Diagram 5-5. AND-OR-Exclusive OR Immediate (Part 1 of 2) (03710) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59		
60		
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	

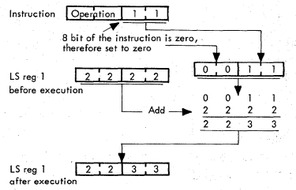


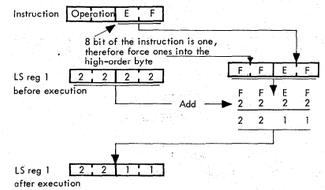
Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▬

● Diagram 5-5. AND-OR-Exclusive OR Immediate (Part 2 of 2) (03710A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

The immediate data byte is added to the halfword in the 'to reg'. The result is set into the 'to reg'.

For subtraction the immediate data byte must be in two's complement (high-order bit on). If so, the immediate data byte is extended to a halfword by high-order ones.





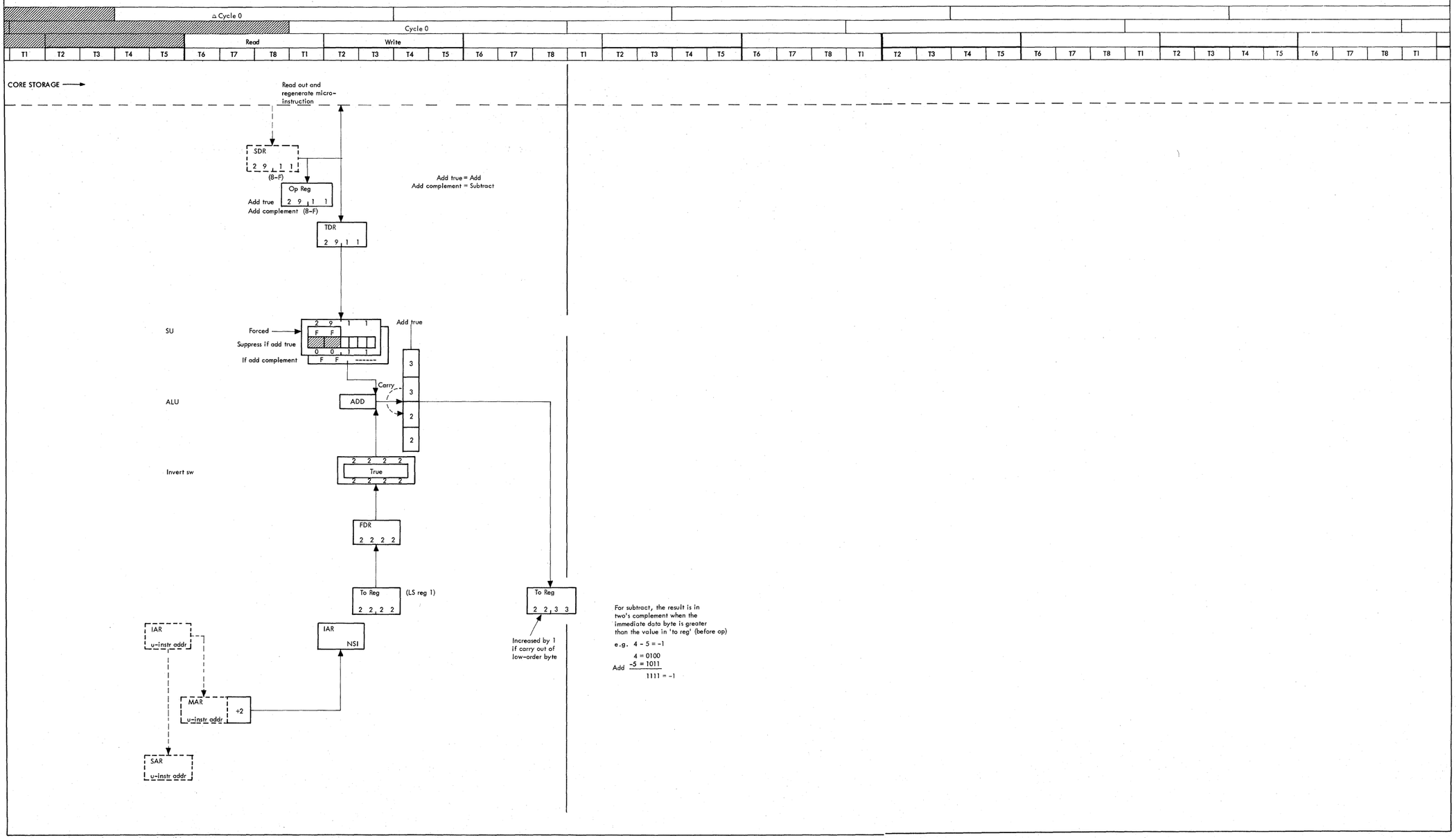
No condition code is set
No carry will be stored
Overflow condition is not indicated

Microinstruction Layout

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Op Code					To Reg			Immediate Data							
2				1											

Mnemonic
ADDI
Format
RI
Type

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
2911	ADDI	1,X'11'	R1*=R1+'0011'
	ADDI	1,-1	R1*=R1+'FFFF'



For subtract, the result is in two's complement when the immediate data byte is greater than the value in 'to reg' (before op)

e.g. 4 - 5 = -1

4 = 0100
Add -5 = 1011
1111 = -1

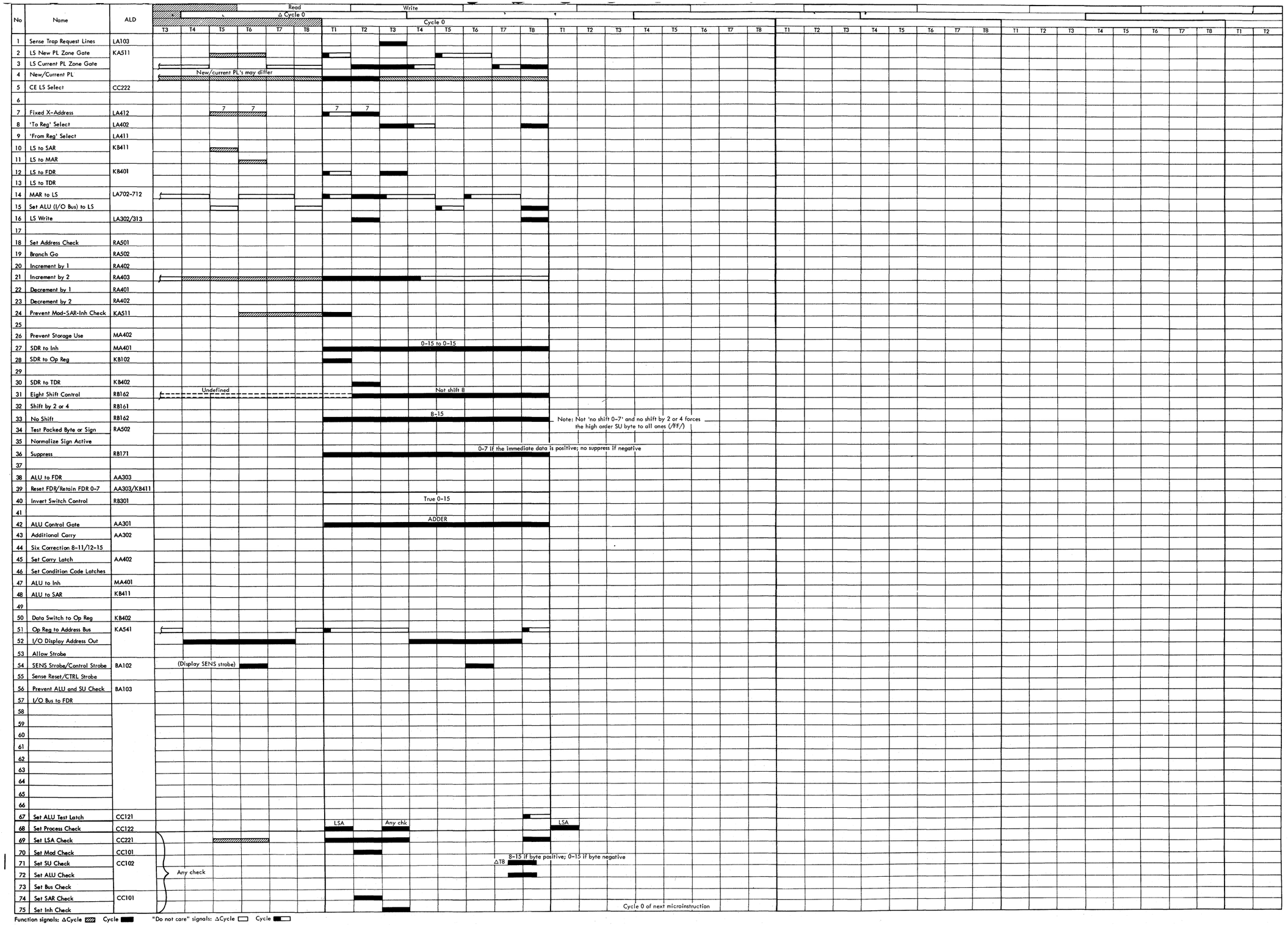
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle

Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

Diagram 5-6. Add Immediate (Part 1 of 2) (03711) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59		
60		
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



● Diagram 5-6. Add Immediate (Part 2 of 2) (03711A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

The immediate data byte is used as a mask. Turned on bits in the mask test the corresponding bits in the low-order byte of the 'to reg' for being off.

The next sequential micro-instruction is skipped:

1. If TMSZ, when all tested bits are off.
2. If TMS, when any tested bit is on.

IAR address of the TMSZ instruction: 0 1 0 2

Instruction

Example 1: Unsuccessful TMSZ

Operation: 3 F

F 9 F 3

LS reg 1 LS reg remain unchanged

Cleared to zero

AND

IAR 0 1 0 4

0 0 3 3

Result is not zero. Continue with NSI, Address 0104.

(Example not shown in the Flowchart)

IAR 0 1 0 6

Example 2: Successful TMSZ

Operation: 3 F

3 5 C 0

Cleared to zero

AND

0 0 0 0

Result is zero, i.e. all bits selected by the mask are zero. Skip over the NSI, continue with address 0106.

Microinstruction Layout

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
Op Code					To Reg			Immediate Data (Mask)								
3				0												TMSZ
3				1												TMS

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
313F	TMSZ	1,X'3F'	Skip if R1,A,'003F'=0
393F	TMS	1,X'3F'	Skip if R1,A,'003F',NE,0

Mnemonic
TMSZ
TMS
Format
RI
Type

Δ Cycle 0 | Δ Cycle 2

Cycle 0 | Cycle 2

Read | Write

T1 T2 T3 T4 T5 T6 T7 T8 T1 T2 T3 T4 T5 T6 T7 T8 T1 T2 T3 T4 T5 T6 T7 T8 T1 T2 T3 T4 T5 T6 T7 T8 T1 T2 T3 T4 T5 T6 T7 T8 T1

CORE STORAGE →

Read out and regenerate micro-instruction

SDR 3 1 3 F (9)

Op Reg 3 1 3 F (9)

TMSZ TMS

TDR 3 1 3 F

SU — Suppress: 3 1 3 F / 0 0 3 F

(No action)

No

ALU zero — Yes → ALU test FL

ALU — /003F/ = 0000 0000 0011 1111 AND /35C0/ = 0011 0101 1100 0000 result = 0000 0000 0000 0000

AND — 0 0 0 0 — (Not used)

Invert sw — 3 5 C 0 True 3 5 C 0

FDR 3 5 C 0

To Reg 3 5 C 0 (LSreg 1)

IAR u-instr addr

IAR NSI

MAR u-instr addr +2

SAR u-instr addr

IAR NSI

IAR NSI +2

Yes

ALU test FL: TMSZ - on TMS - off — No — (Not used)

MAR NSI +2

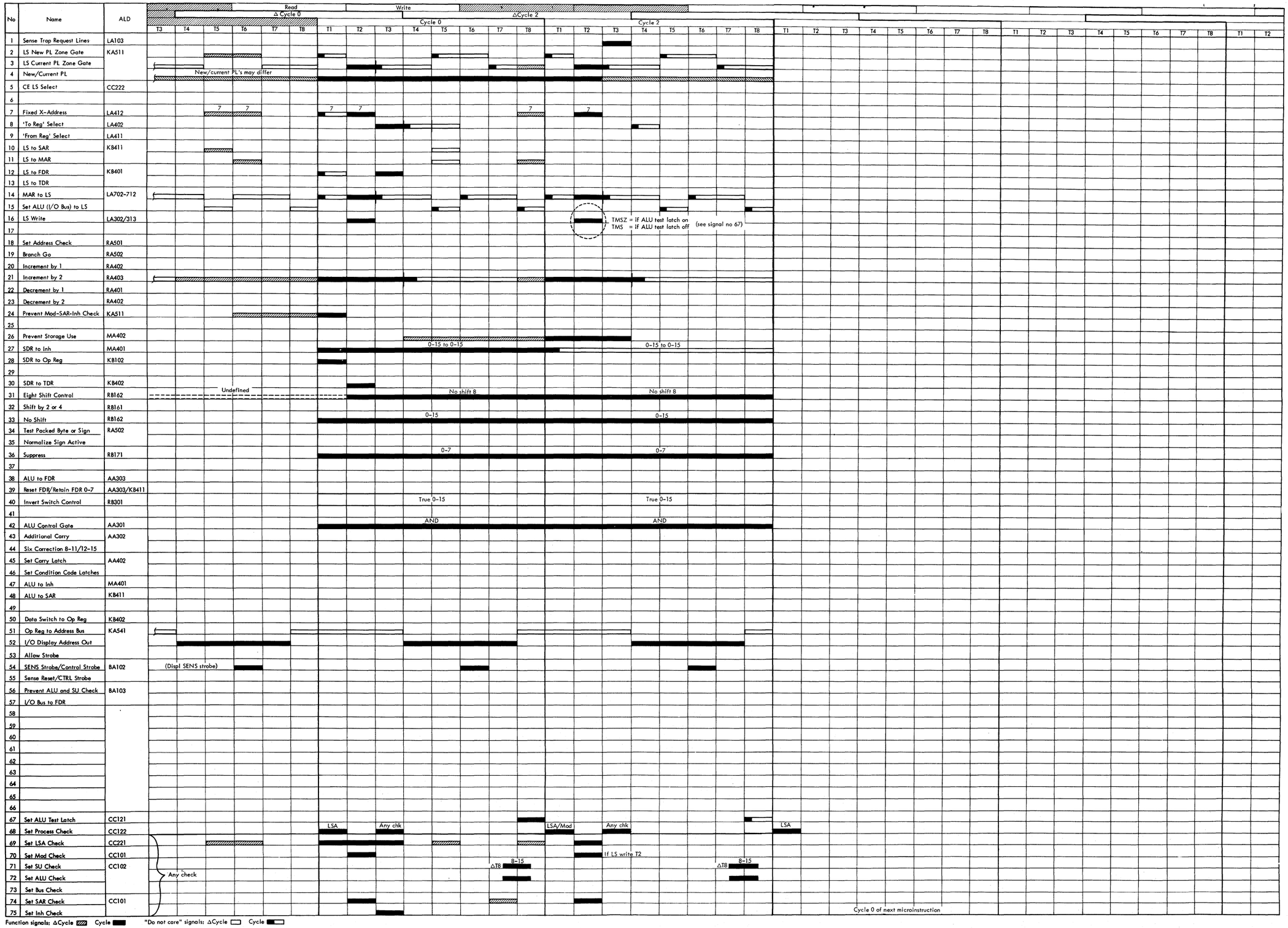
Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle

● Diagram 5-7. Test under Mask and Skip if Zero and Not Zero (Part 1 of 2) (03712A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

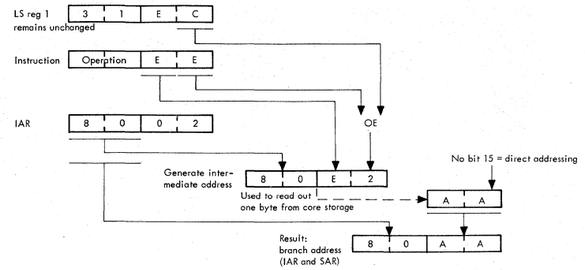
No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59		
60		
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▭

● Diagram 5-7. Test under Mask and Skip if Zero and Not Zero (Part 2 of 2) (03712A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

A branch address is combined with the current block address (high-order byte of IAR) and an even byte is read out by an intermediate address (even byte = direct addressing). The intermediate address consists of the current block address as the high-order byte while the low-order byte is obtained by exclusive ORing the immediate data byte with the low-order four-bit digit (hexadecimal) in the 'to reg'. The 'to reg' remains unchanged.



Microinstruction Layout

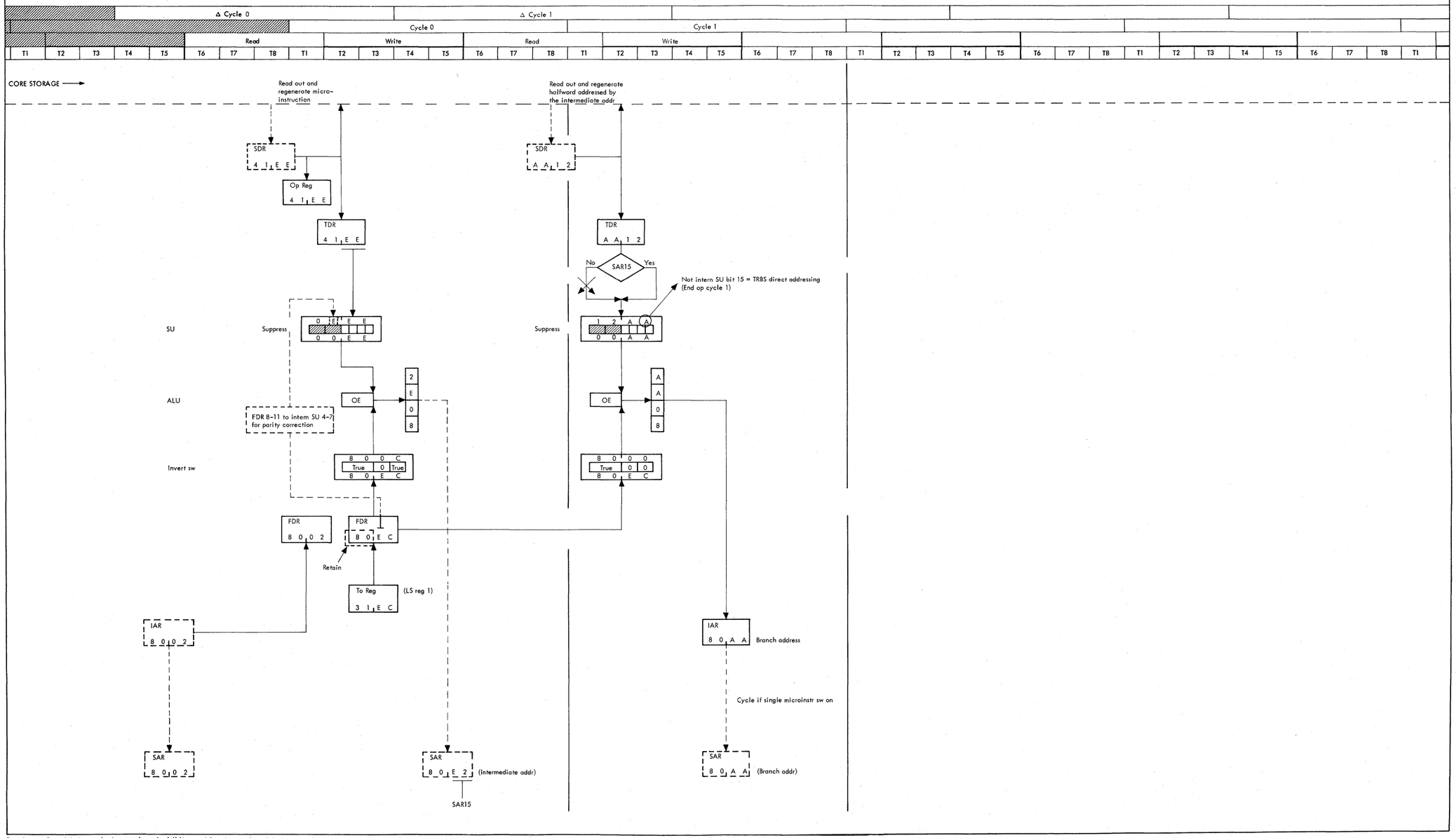
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Op Code					To Reg			Immediate Data (Addr)							
4				0											

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
41EE	TRBS	1, LABEL	BR TO IAR.0-7/BY(IAR.0-7/INST.8-11/X) , X=INST.12-15, OE, R1.12-15, IF BY.15=1 BR INDIR.

Mnemonic
TRBS
Format
RI
Type
Direct Addressing

Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

Diagram 5-8. Translate and Branch Short (Direct Addressing) (Part 1 of 2) (03713) 2020 ≥ 50,000 FEMDM Vol 2 › (8/69)

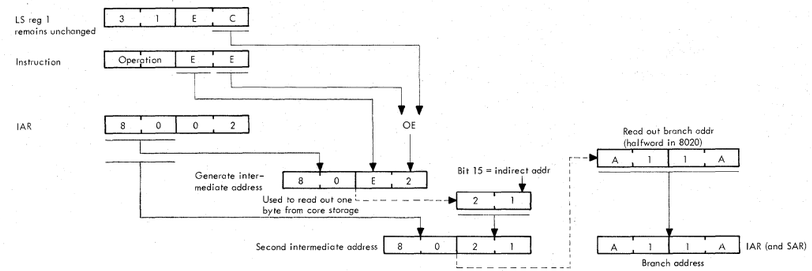
No	Name	ALD	Read Δ Cycle 0 T3	T4	T5	T6	T7	T8	Write Cycle 0 T1	T2	T3	T4	T5	T6	T7	T8	Read Δ Cycle 1 T1	T2	T3	T4	T5	T6	T7	T8	Write Cycle 1 T1	T2	T3	T4	T5	T6	T7	T8
1	Sense Trap Request Lines	LA103																														
2	LS New PL Zone Gate	KA511																														
3	LS Current PL Zone Gate																															
4	New/Current PL			New/current PL's may differ																												
5	CE LS Select	CC222																														
6																																
7	Fixed X-Address	LA412			7	7			7	7						1		1			7			7								
8	'To Reg' Select	LA402																														
9	'From Reg' Select	LA411																														
10	LS to SAR	KB411																														
11	LS to MAR																															
12	LS to FDR	KB401																														
13	LS to TDR																															
14	MAR to LS	LA702-712																														
15	Set ALU (I/O Bus) to LS																															
16	LS Write	LA302/313																														
17																																
18	Set Address Check	RA501																														
19	Branch Go	RA502																														
20	Increment by 1	RA402																														
21	Increment by 2	RA403																														
22	Decrement by 1	RA401																														
23	Decrement by 2	RA402																														
24	Prevent Mod-SAR-Inh Check	KA511																														
25																																
26	Prevent Storage Use	MA402																														
27	SDR to Inh	MA401										0-15 to 0-15										0-15 to 0-15										
28	SDR to Op Reg	KB102																														
29																																
30	SDR to TDR	KB402																														
31	Eight Shift Control	RB162	Undefined								No shift 8 (TDR 8-15 to SU 8-15 only)										No shift 8 if SAR 15; cross shift if no SAR 15											
32	Shift by 2 or 4	RB161																														
33	No Shift	RB162										0-15										0-15										
34	Test Packed Byte or Sign	RA502																														
35	Normalize Sign Active																															
36	Suppress	RB171										0-7										0-7										
37																																
38	ALU to FDR	AA303																														
39	Reset FDR/Retain FDR 0-7	AA303/KB411									Retain FDR 0-7																					
40	Invert Switch Control	RB301									True 0-15, invert 8-11 = /true 0 true/										True 0-15, invert 8-15 = /true 00/										
41																																
42	ALU Control Gate	AA301												OE										OE								
43	Additional Carry	AA302																														
44	Six Correction 8-11/12-15																															
45	Set Carry Latch	AA402																														
46	Set Condition Code Latches																															
47	ALU to Inh	MA401																														
48	ALU to SAR	KB411																														(Cycle depending if Single Microinstruction switch on)
49																																
50	Data Switch to Op Reg	KB402																														
51	Op Reg to Address Bus	KA541																														
52	I/O Display Address Out																															
53	Allow Strobe																															
54	SENS Strobe/Control Strobe	BA102		(Displ SENS strobe)																												
55	Sense Reset/CTRL Strobe																															
56	Prevent ALU and SU Check	BA103																														
57	I/O Bus to FDR																															
58																																
59																																
60																																
61																																
62																																
63																																
64																																
65																																
66																																
67	Set ALU Test Latch	CC121																														
68	Set Process Check	CC122							LSA		Any chk							LSA/Mod		Any chk						LSA						
69	Set LSA Check	CC221																														
70	Set Mod Check	CC101																														
71	Set SU Check	CC102											8-15										8-15									
72	Set ALU Check		Any check																													
73	Set Bus Check																															
74	Set SAR Check	CC101																														
75	Set Inh Check																															Cycle 0 of next microinstruction

Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▭

● Diagram 5-8. Translate and Branch Short (Direct Addressing) (Part 2 of 2) (03713A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

This operation is similar to that described in Diagram 5-8, except that the resulting branch address is used as a second intermediate address if the byte read out by the first intermediate address is odd (bit 15 on).

The second intermediate address reads out a halfword used as branch address.

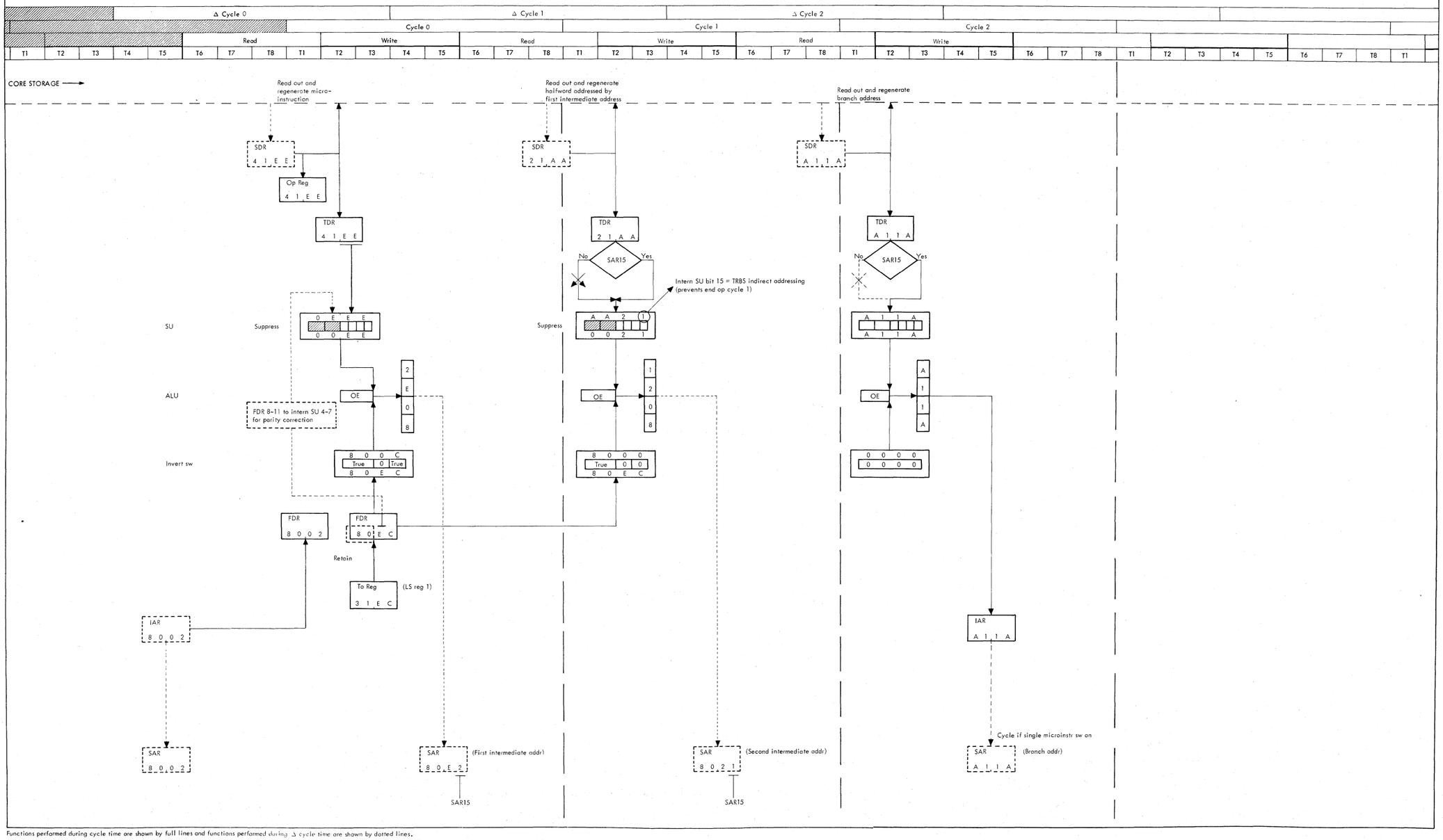


Microinstruction Layout

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Op Code					To Reg			Immediate Data (Addr)							
4				0											

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
41EE	TRBS	1,LABEL	BR TO IAR.0-7/BY(IAR.0-7/INST.8-11/X) ,; X=INST.12-15,OE,R1.12-15, IF BY.15=1 BR INDIR.

Mnemonic
TRBS
Format
RI
Type
Indirect Addressing



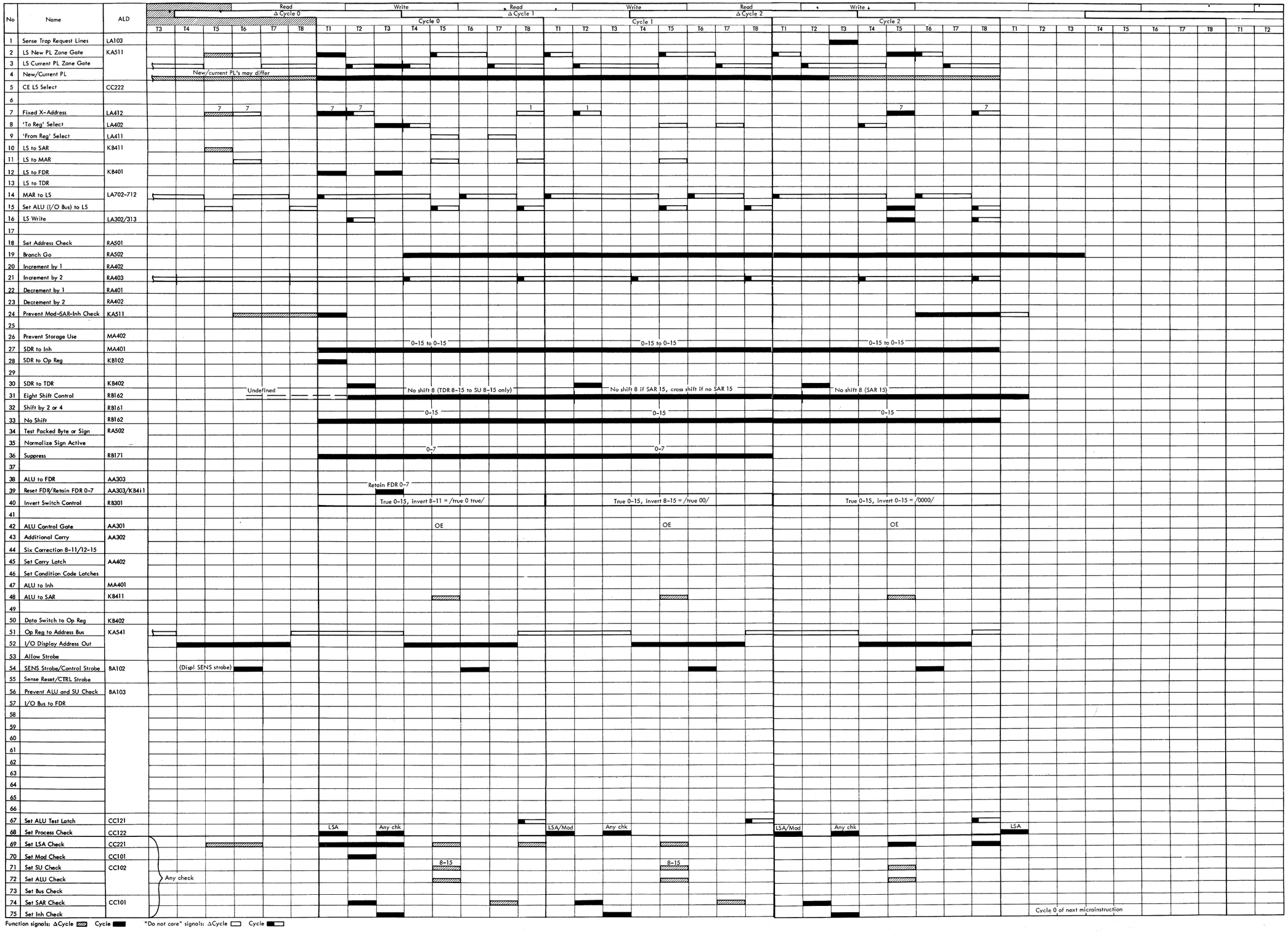
Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle

Diagram 5-9. Translate and Branch Short'(Indirect Addressing) (Part 1 of 2) (03714) 2020 ≥ 50,000 FEMDM Vol 2 › (8/69)

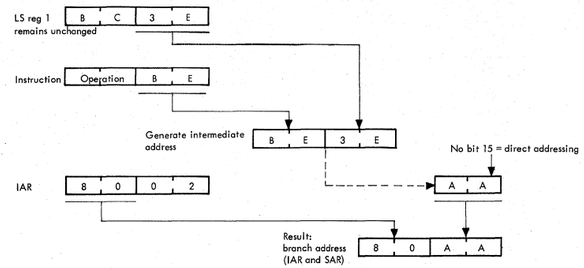
No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB4i1
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59		
60		
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



● Diagram 5-9. Translate and Branch Short (Indirect Addressing) (Part 2 of 2) (03714A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

A branch address is combined with the current block address and an even byte read out by an intermediate address (even byte = direct addressing).

The intermediate address consists of the immediate data byte as block address and the low-order byte of the 'to reg'. The 'to reg' remains unchanged.



Microinstruction Layout

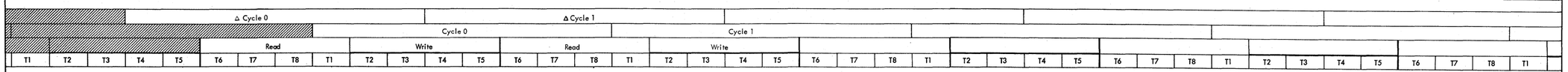
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Op Code					To Reg			Immediate Data (Addr)							
4				1											

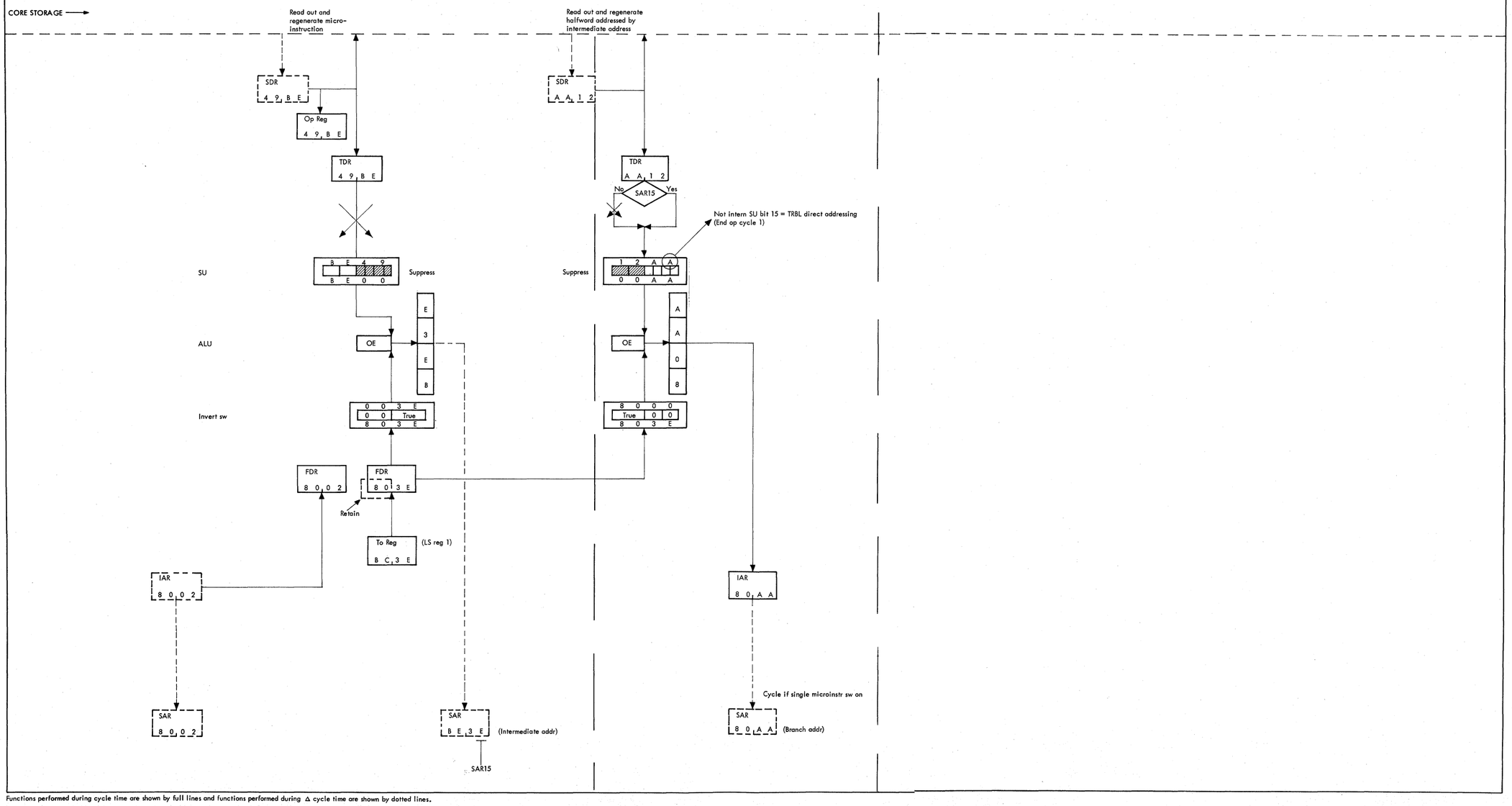
Mnemonic
TRBL
Format
RI
Type
Direct Addressing

```
INST     MNEM  OPERANDS      STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
49BE     TRBL  1,B(LABEL)    BR TO IAR.0-7/BY(INST.8-15/R1.8-15), IF BY.15=1 BR INDIR.
```

Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
- ΔCycle
- Cycle

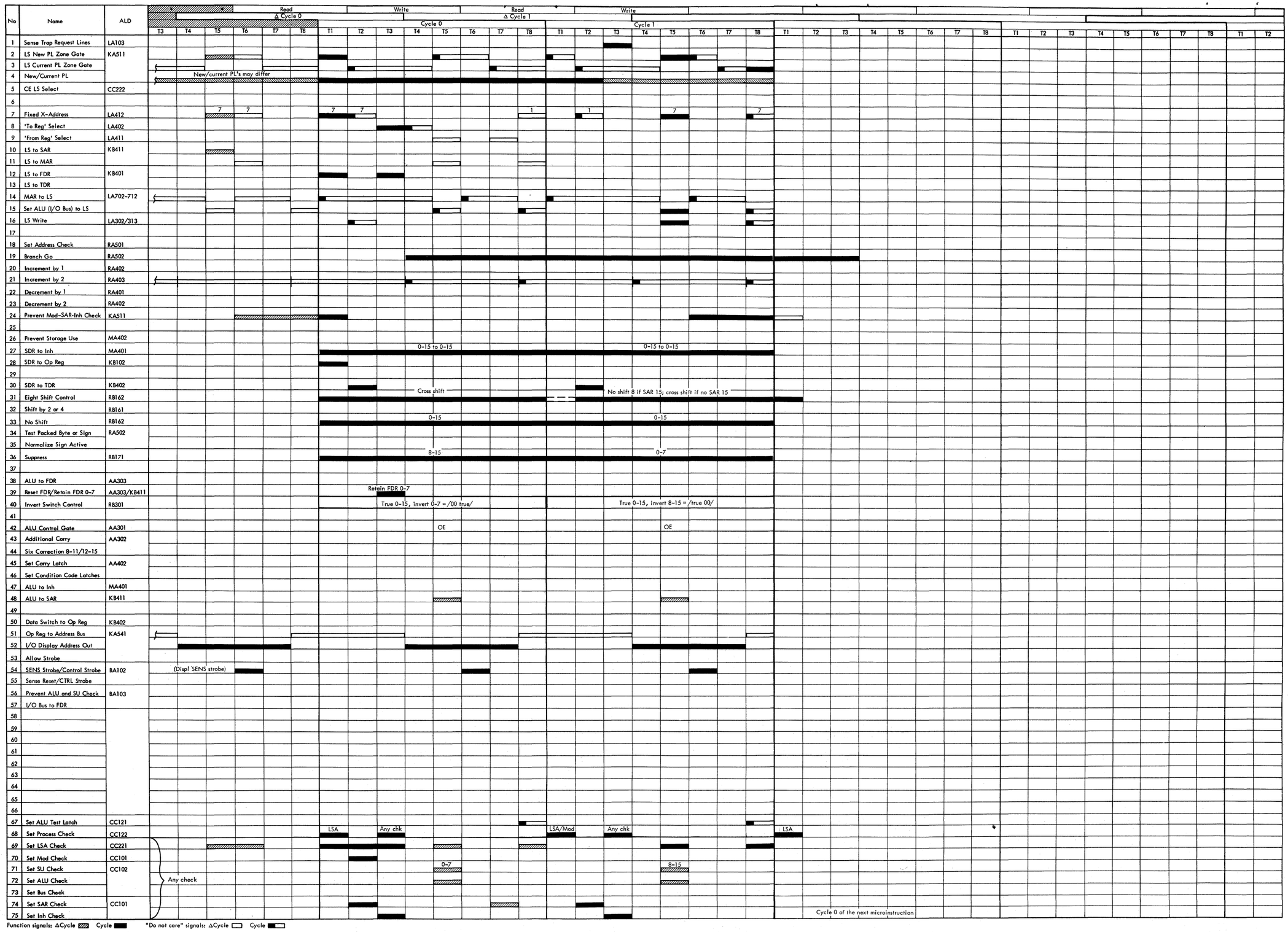




Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

Diagram 5-10. Translate and Branch Long (Direct Addressing) (Part 1 of 2) (03715A) 2020 ≥ 50,000 FEMDM Vol 2* (8/69)

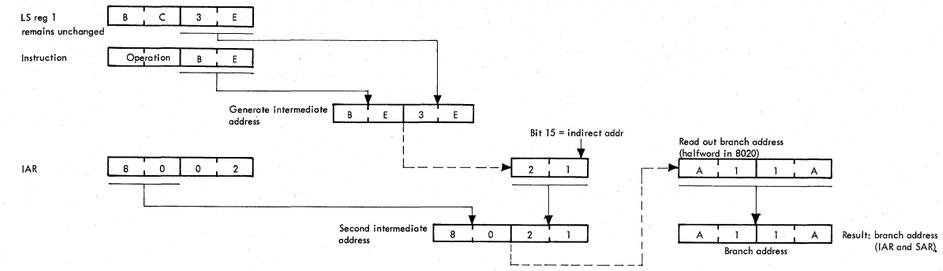
No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59		
60		
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▬

This operation is similar to that described in Diagram 5-10, part 1, except that the resulting branch address is used as second intermediate address if the byte read out by the first intermediate address is odd (bit 15 on).

The second intermediate address reads out a halfword used as branch address.

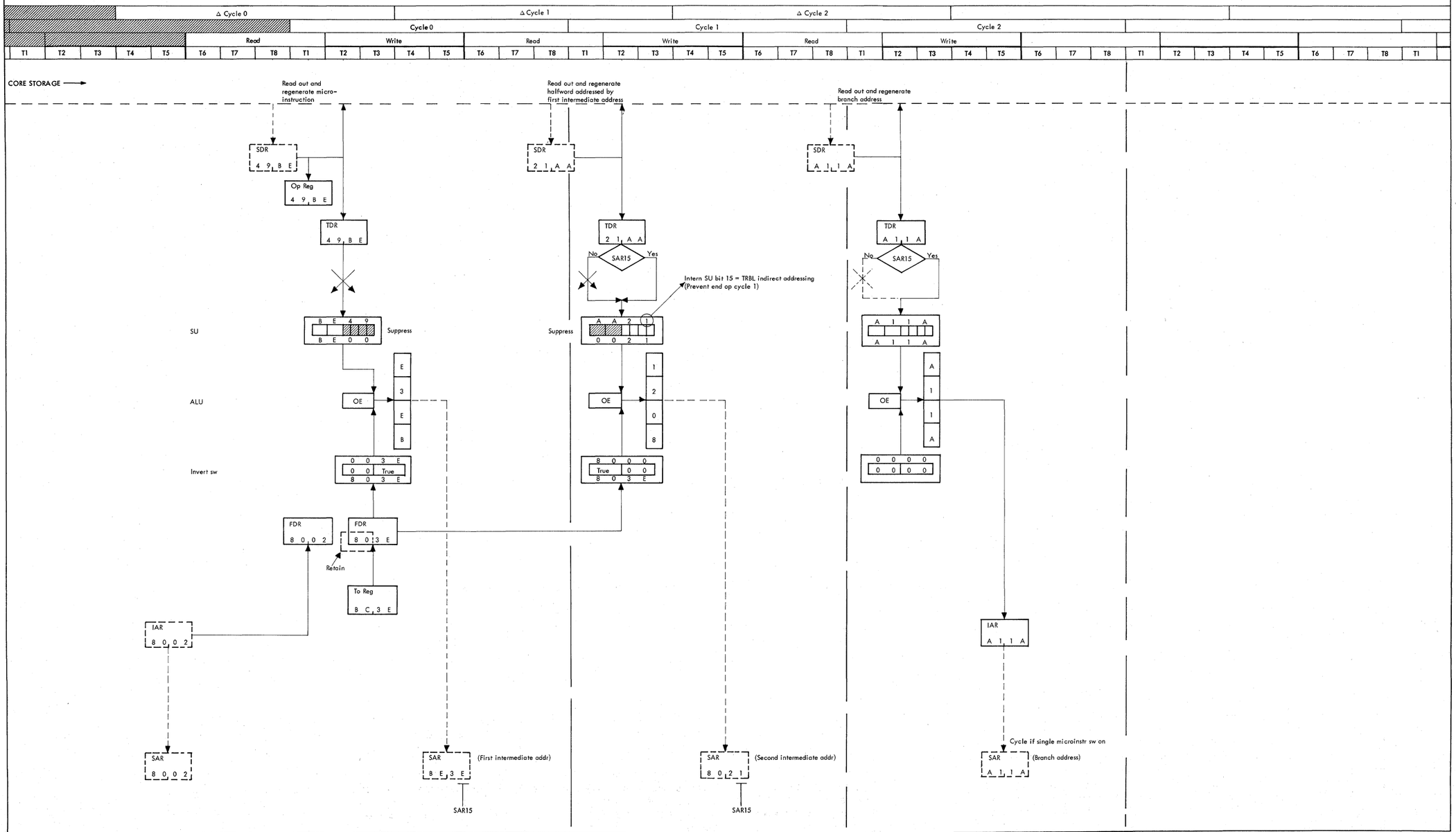


Microinstruction Layout

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Op Code					To Reg			Immediate Data (Addr)							
4				1											

Mnemonic
TRBL
Format
RI
Type
Indirect Addressing

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
49BE	TRBL	1,B(LABEL)	BR TO IAR.0-7/BY(INST.8-15/R1.8-15), IF BY.15=1 BR INDIR.



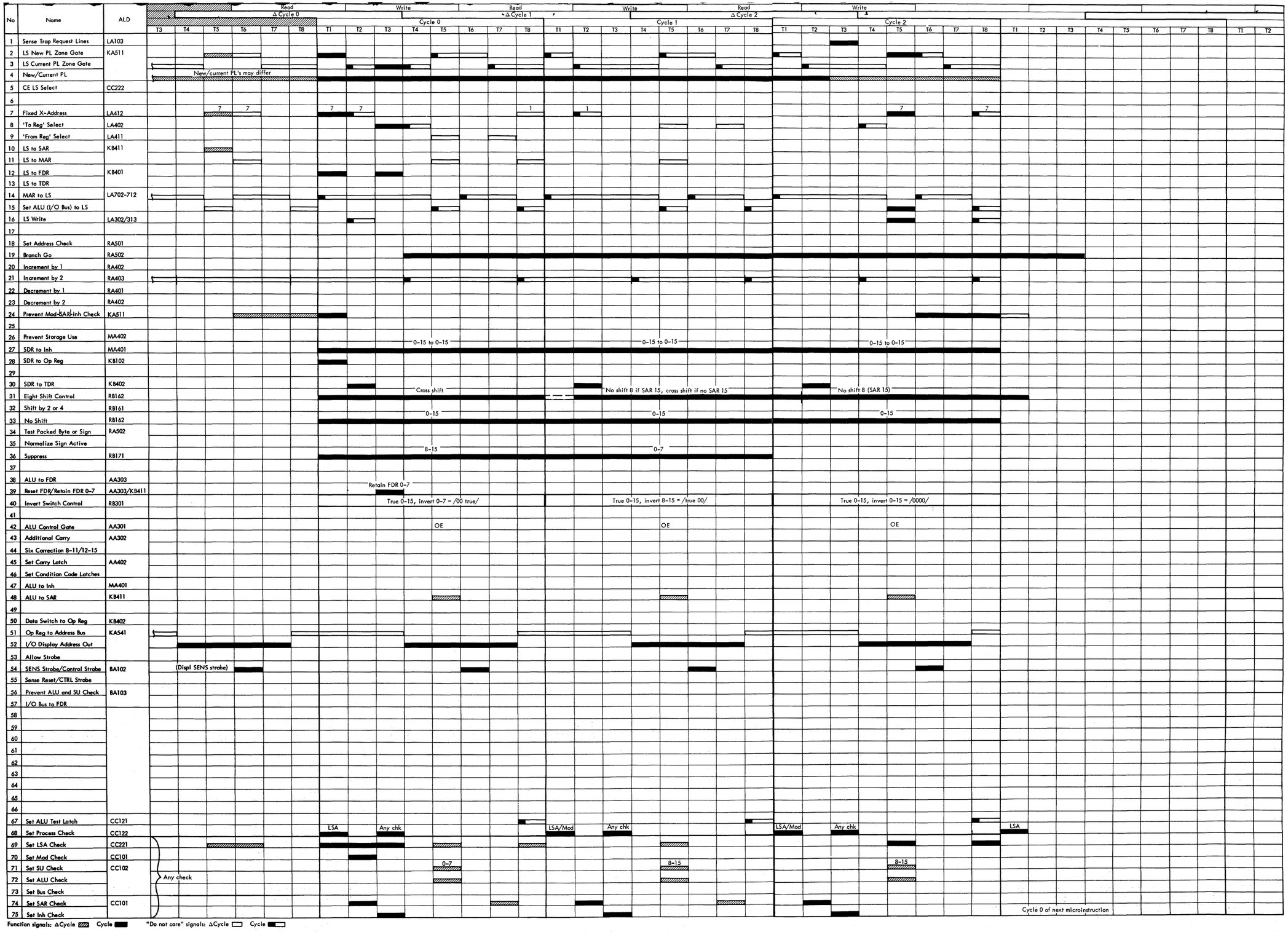
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
- Δ Cycle
- Cycle

Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

Diagram 5-11. Translate and Branch Long (Indirect Addressing) (Part 1 of 2) (03716A) 2020 ≥ 50,000 FEMDM Vol•2 (8/69) •

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59		
60		
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



● Diagram 5-11. Translate and Branch Long (Indirect Addressing) (Part 2 of 2) (03716A)

A halfword, read out by an address comprising a combination of the current block address and the displacement address (low-order byte), is loaded into 'to reg'.

No loading is performed if 'to reg' = LS register 7 (IAR).

Instruction: Operation | A | A

IAR: 8 | 0 | 0 | 2

Generate halfword address: 8 | 0 | A | A

LS reg 1 before execution: 1 | 2 | 3 | 4

Read out halfword to be loaded: A | B | C | D

Remains unchanged

LS reg 1 after execution: A | B | C | D

Microinstruction Layout

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Op Code					To Reg			Displacement Addr							
.5				0											0

Indicates Direct addressing

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
51AA	LH	1,LABEL	R1=HW(IAR.0-7/INST.8-14)

Mnemonic
LH
Format
RD
Type
Direct Addressing

Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
- ΔCycle
- Cycle

Δ Cycle 0 | Δ Cycle 2

Cycle 0 | Cycle 2

Read | Write | Read | Write

T1 T2 T3 T4 T5 T6 T7 T8 T1 T2 T3 T4 T5 T6 T7 T8 T1 T2 T3 T4 T5 T6 T7 T8 T1 T2 T3 T4 T5 T6 T7 T8 T1 T2 T3 T4 T5 T6 T7 T8 T1

CORE STORAGE

Read out and regenerate micro-instruction

Read out and regenerate halfword to be loaded into 'to reg'

SDR 5 1 A A

Op Reg 5 1 A A

TDR 5 1 A A

Not op reg bit 15 = direct addr

SU — Suppress: 5 1 A A / 0 0 A A

ALU — OE → A A 0 8

Invert sw: 8 0 0 0 / True 0 0 / 8 0 0 2

FDR 8 0 0 2

IAR 8 0 0 2

IAR 8 0 0 4 (NSI)

MAR 8 0 0 2 -2

SAR 8 0 0 2

SAR 8 0 A A

SDR A B C D

TDR A B C D

A B C D / A B C D

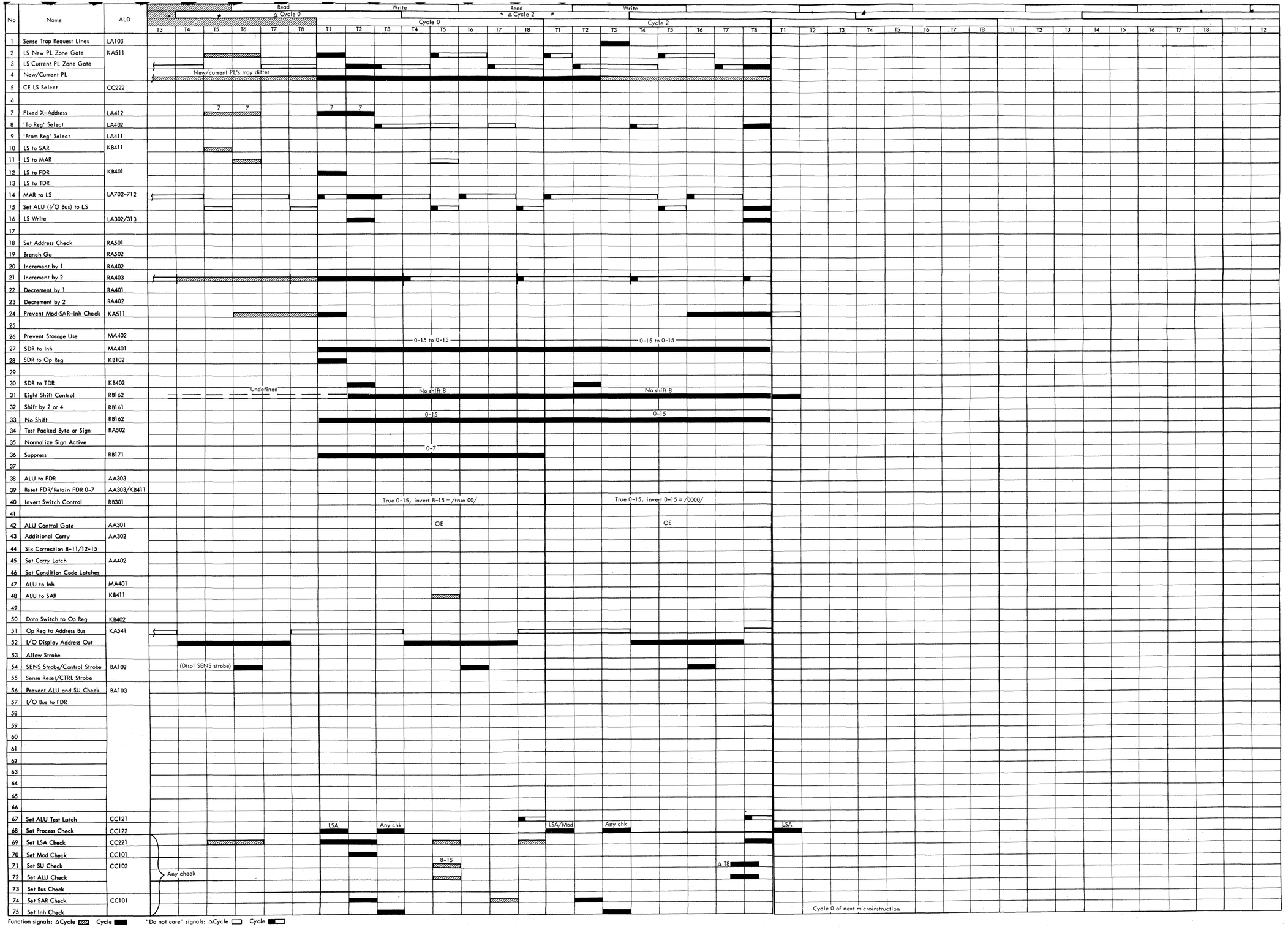
OE → D C B A

0 0 0 0 / 0 0 0 0

To Reg A B C D (LS reg 1)

Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59		
60		
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	

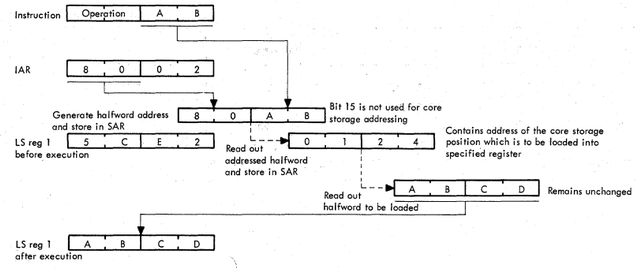


Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▭

● Diagram 5-12. Load Halfword (Direct Addressing) (Part 2 of 2) (03717A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

A halfword is read out and loaded into the 'to reg' (not if 'to reg' = LS register 7, IAR).

The halfword address was previously read out by an address comprising a combination of the current block address and the displacement address (low-order byte).



Microinstruction Layout

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Op Code					To Reg			Displacement Addr							
5				0											1

Indicates indirect addressing

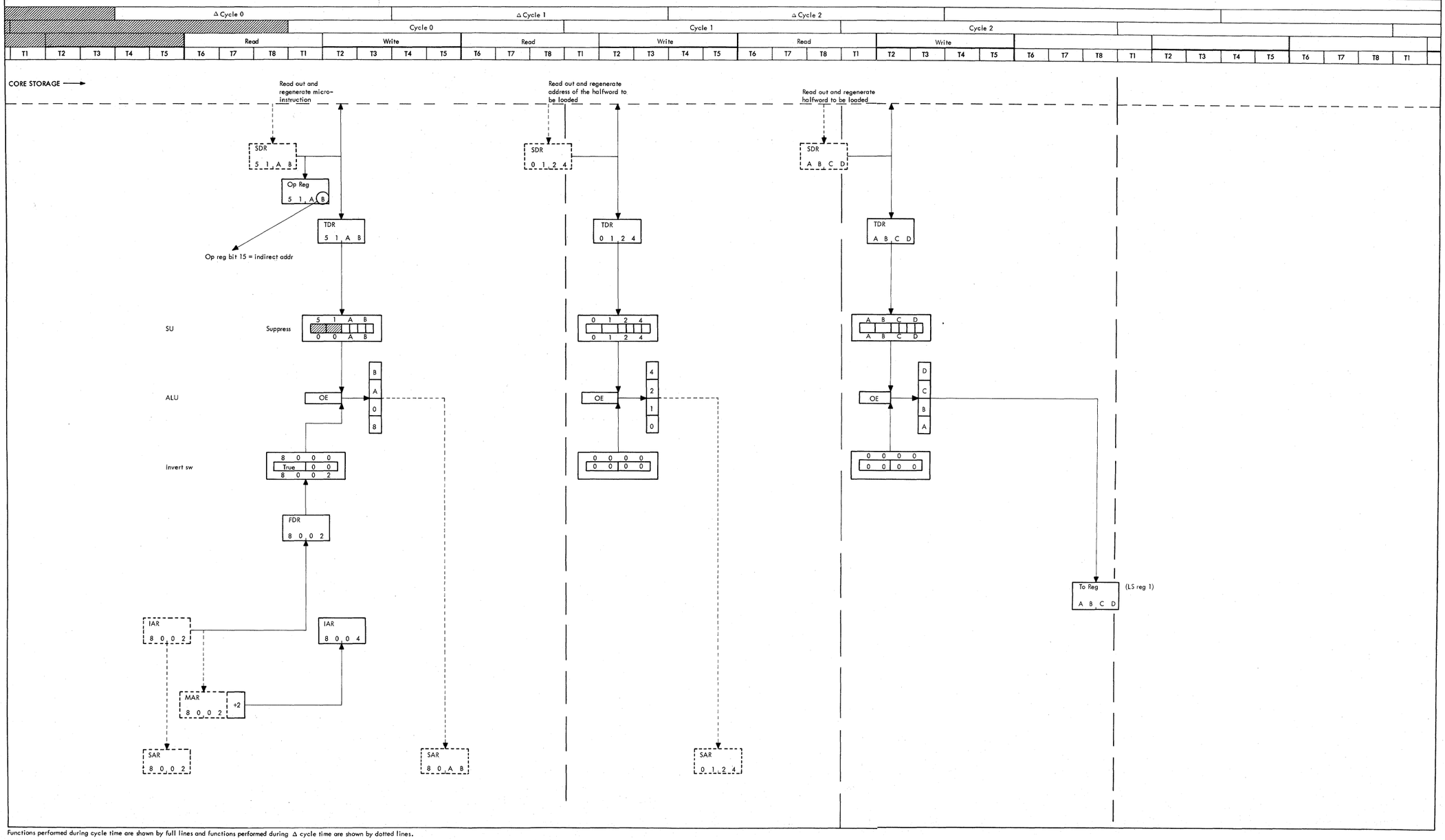
Mnemonic
LH
Format
RD
Type
Indirect Addressing

INST MNEM OPERANDS STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX

51AB LH 1,LABEL,I R1*=HW(HW(IAR.0-7/INST.8-14))

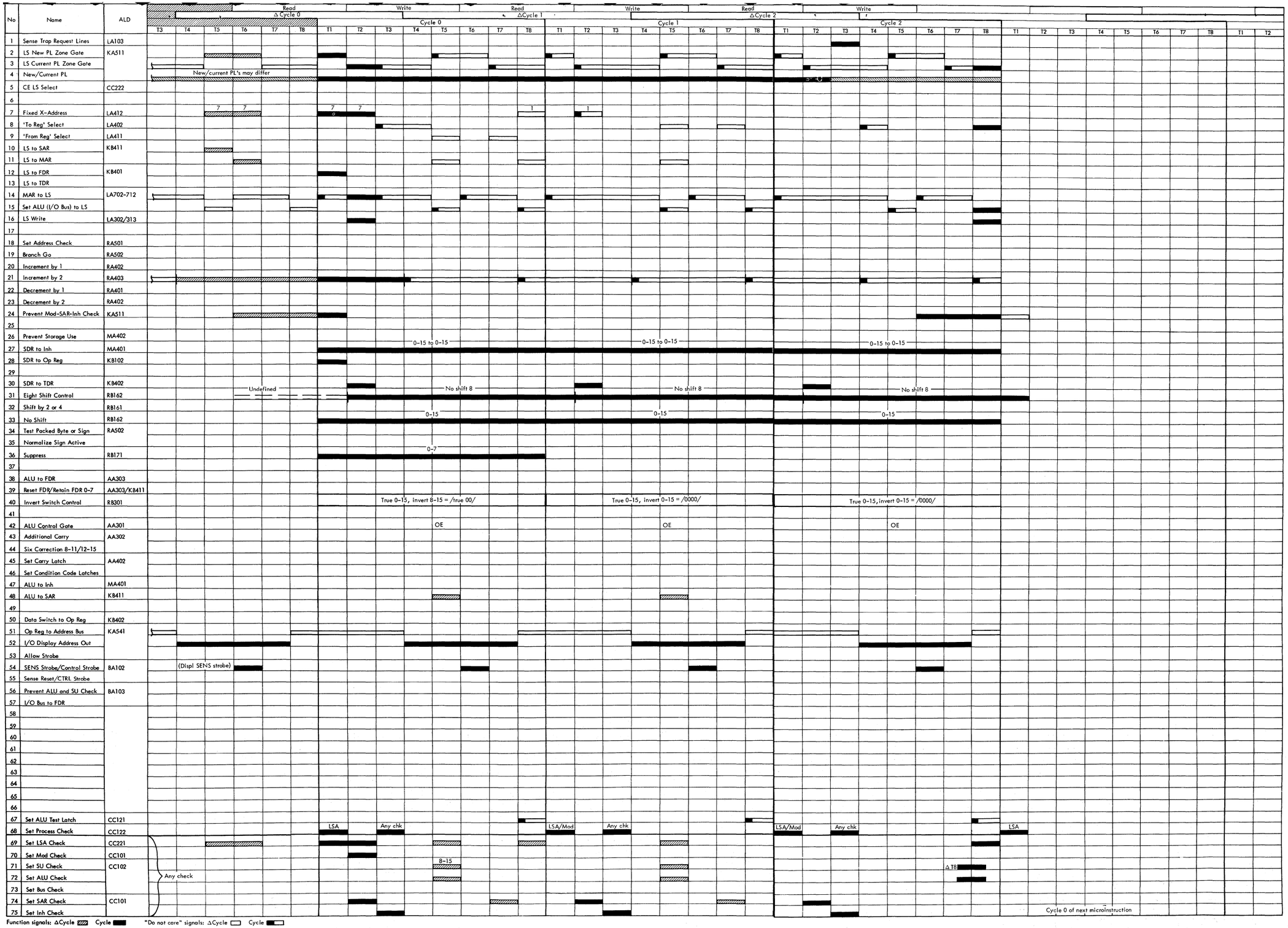
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

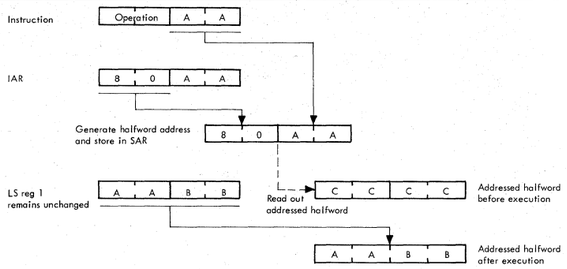
No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59		
60		
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▭

● **Diagram 5-13. Load Halfword (Indirect Addressing) (Part 2 of 2)** (03718A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

The 'to reg' halfword is stored in core storage. The address comprises a combination of the current block address and the displacement address (low-order byte).



Microinstruction Layout

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Op Code					To Reg			Displacement Addr							
5				1											0

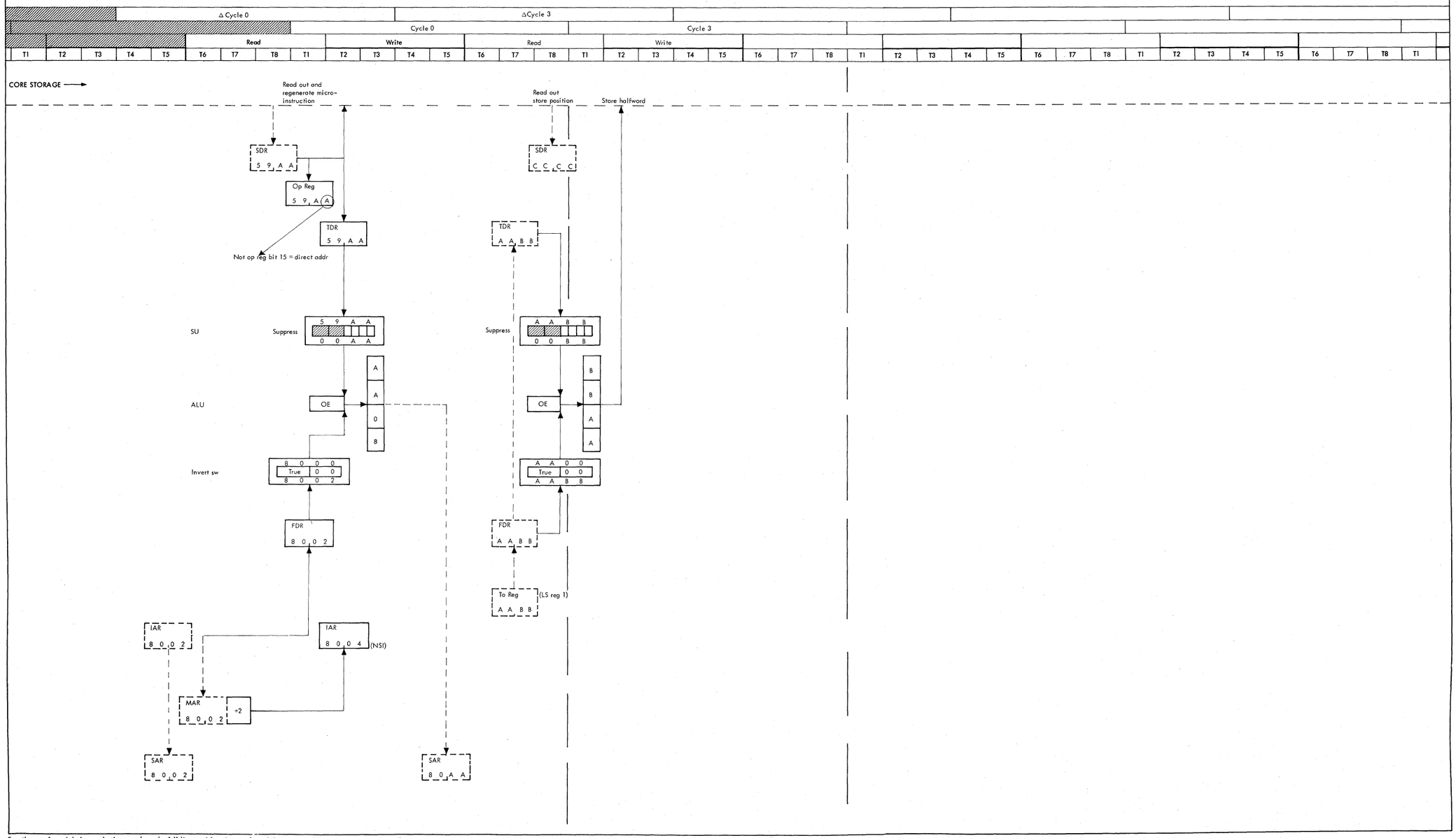
Indicates direct addressing

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
59AA	STH	1,LABEL	HW(IAR.0-7/INST.8-14)*=R1

Mnemonic: STH

Format: RD

Type: Direct Addressing



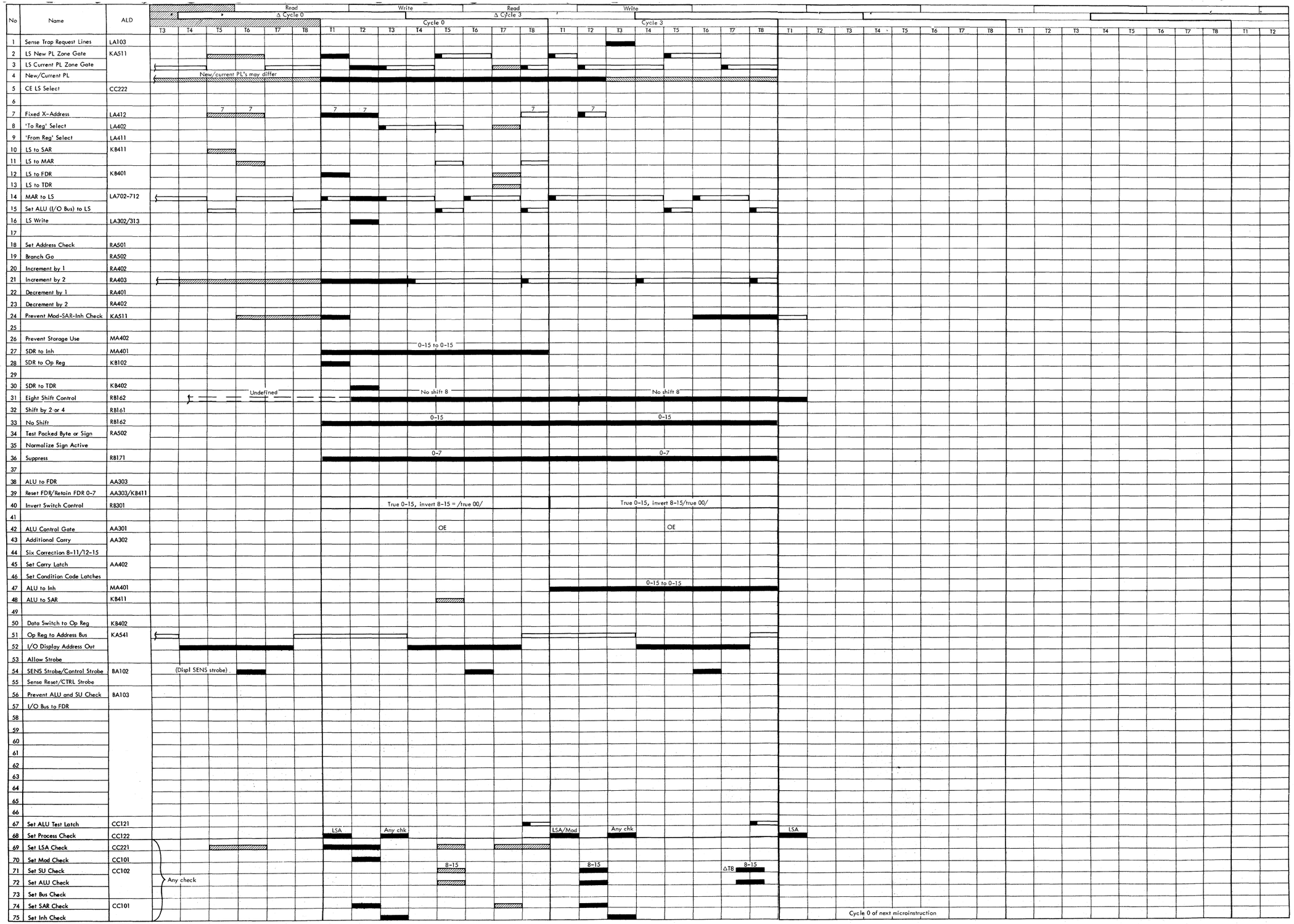
Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle

Diagram 5-14. Store Halfword (Direct Addressing) (Part 1 of 2) (03719) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

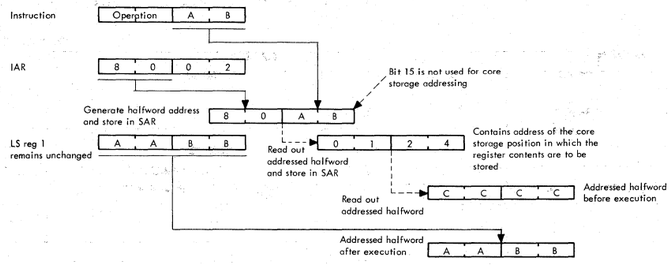
No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59		
60		
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▭

● Diagram 5-14. Store Halfword (Direct Addressing) (Part 2 of 2) (03719A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

The 'to reg' halfword is stored into core storage. The store address was previously read out by an address comprising a combination of the current block address and the displacement address (low-order byte).



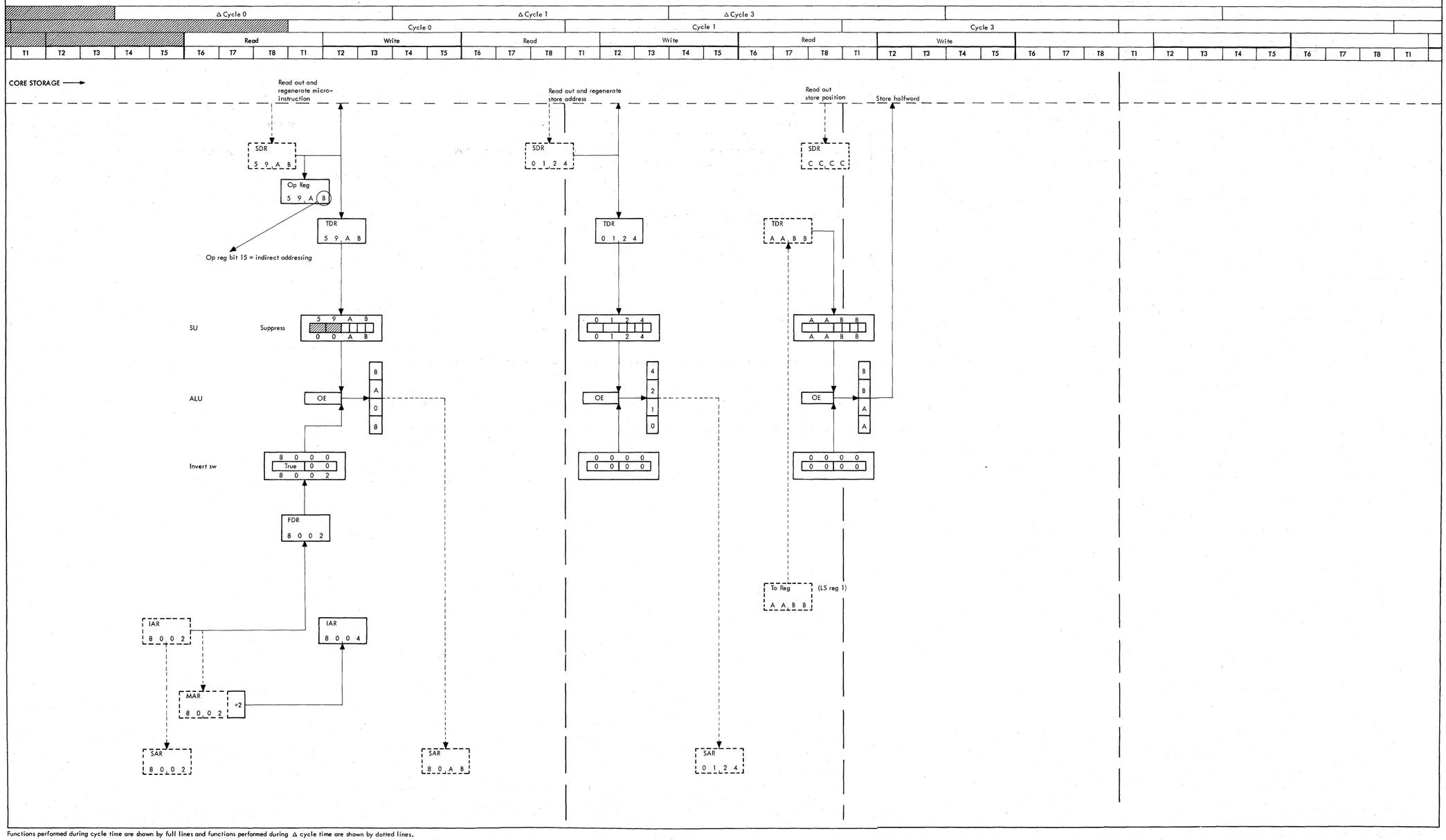
Microinstruction Layout

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Op Code					To Reg			Displacement Addr							
5				1											1

Indicates indirect addressing

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
59AB	STH	1,LABEL,I	HW(HW(IAR.0-7/INST.8-14))=R1

Mnemonic
STH
Format
RD
Type
Indirect Addressing

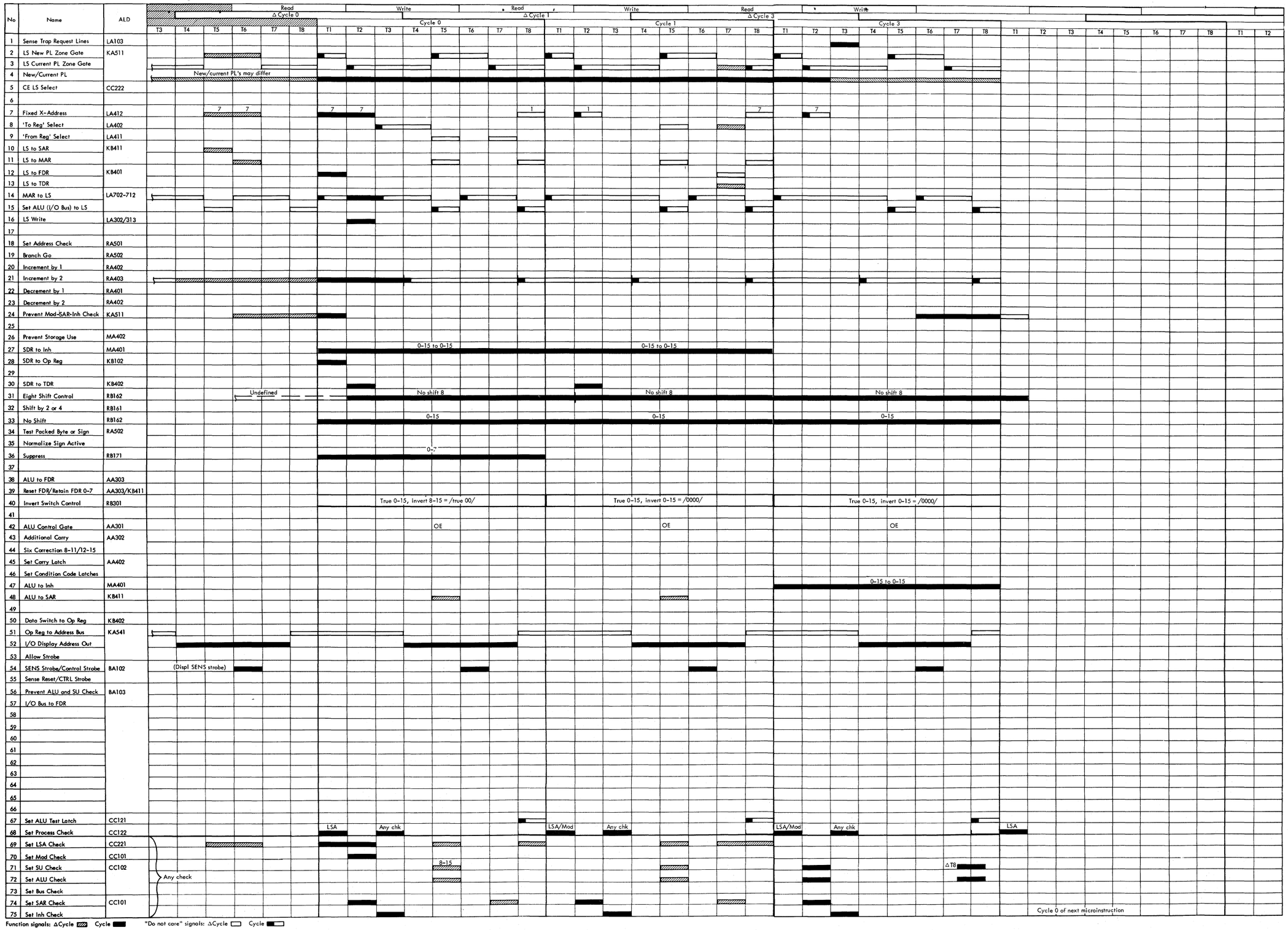


Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

Note: For "Do not care" functions refer to timing chart below.

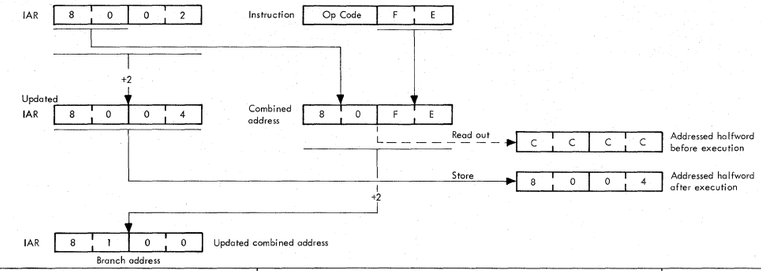
"Do not care" signals:
ΔCycle
Cycle

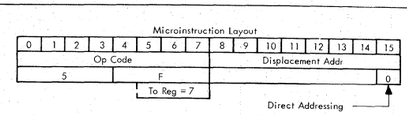
No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59		
60		
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▬

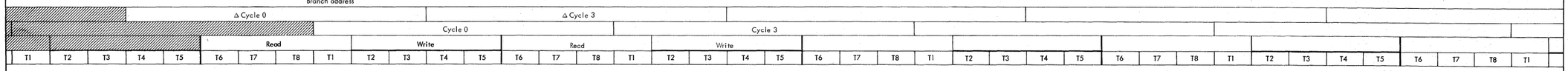
The updated microinstruction address (IAR + 2) is stored in core storage. The store address comprises a combination of the current block address and the displacement address (low-order byte). The store address is incremented by 2 and used to read out the next microinstruction (branch to store address + 2). The contents of LS register 4 are destroyed.

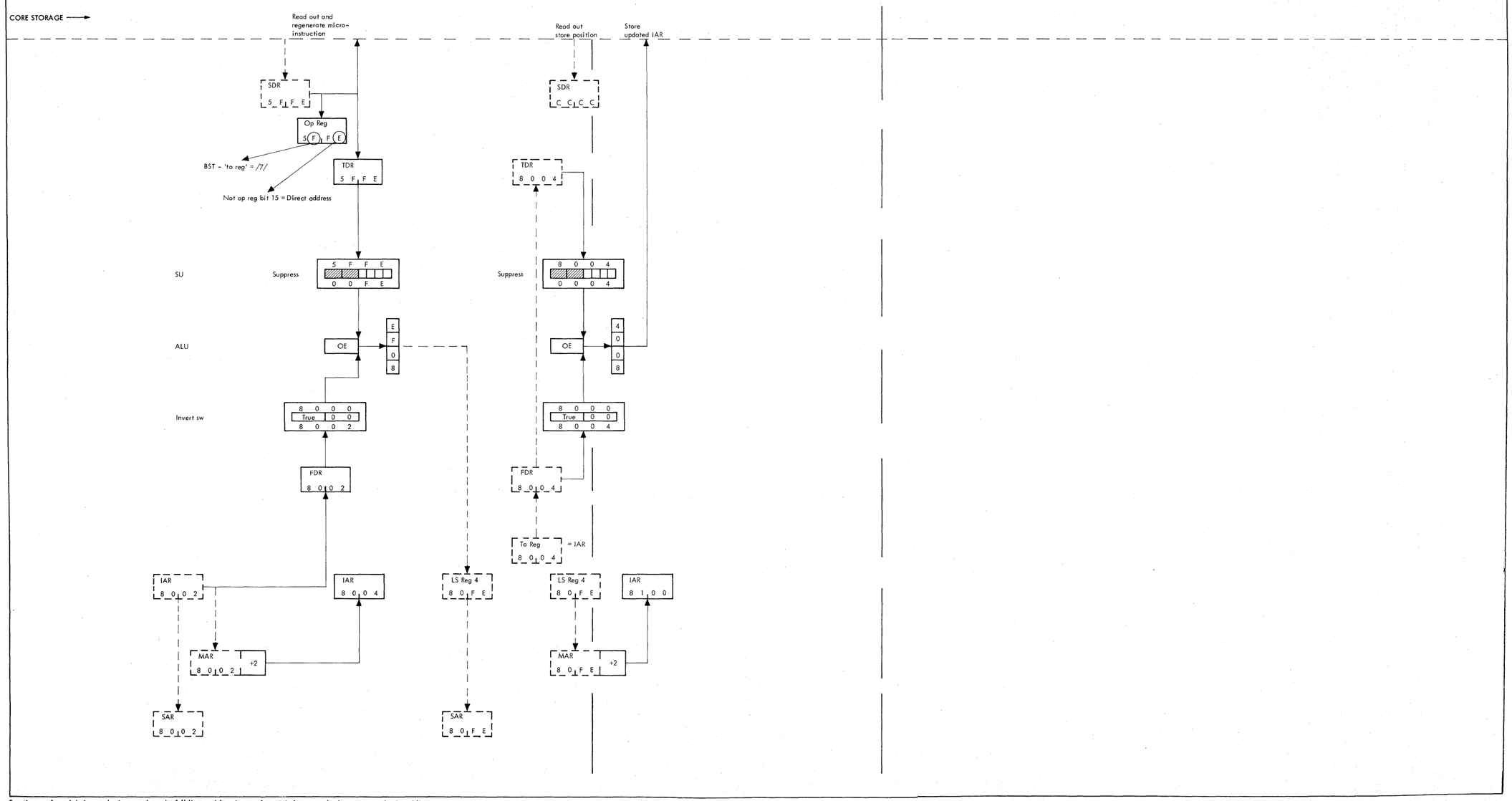




Mnemonic
BST
Format
RD
Type
Direct Addressing

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
5FFE	BST	LABEL	HW(IAR.0-7/INST.8-14)#=R7,BR TO HW (IAR.0-7/INST.8-14)+2



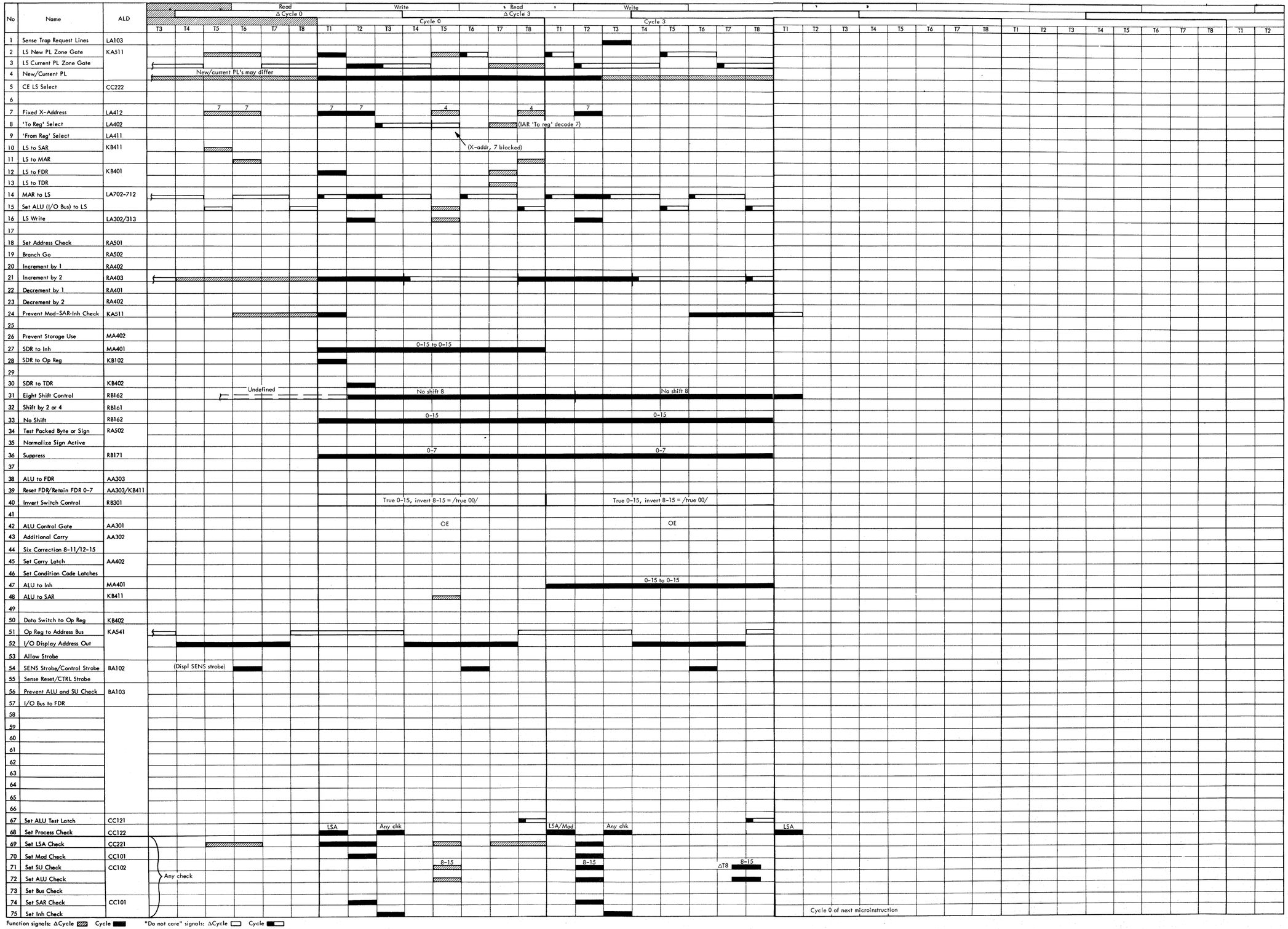


Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle

Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

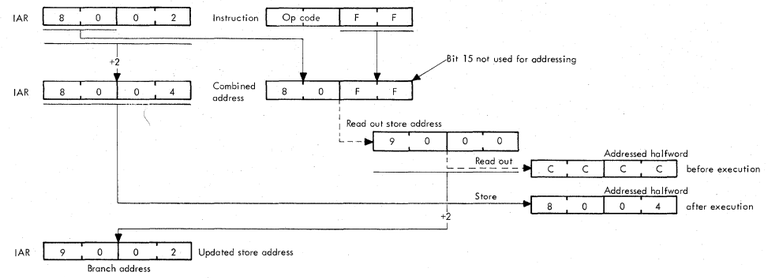
No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59		
60		
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	

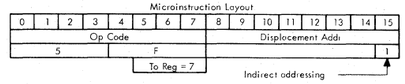


Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▭

● Diagram 5-16. Branch and Store (Direct Addressing) (Part 2 of 2) (03721A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

The updated microinstruction address (IAR + 2) is stored in core storage.
The store address is read out by an address comprising a combination of the current block address and the displacement address (low-order byte).
The store address is incremented by 2 and used to read out the next microinstruction (branch to store address + 2). The contents of LS register 4 are destroyed.





Mnemonic
BST
Format
RD
Type
Indirect Addressing

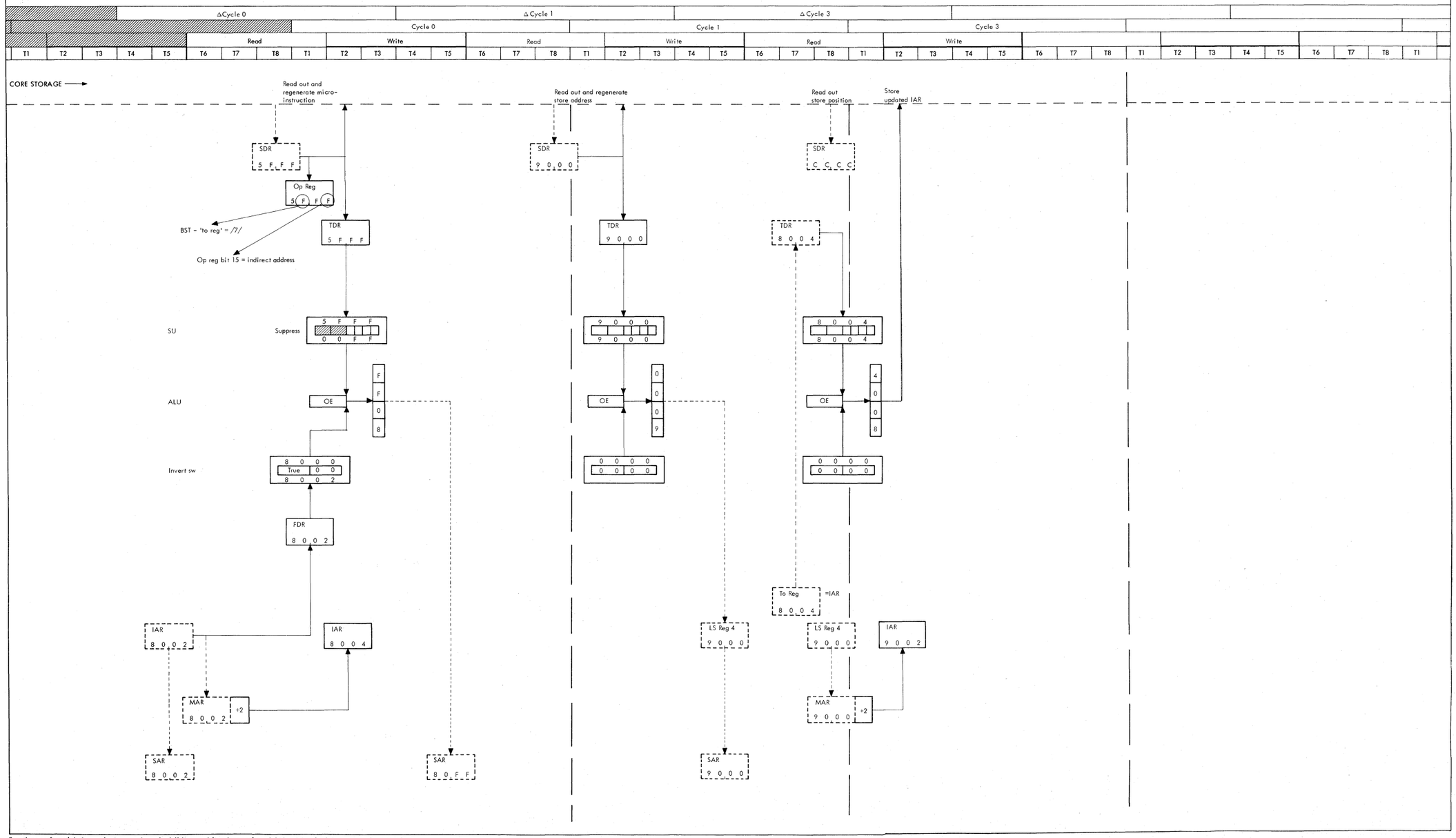
INST 5FFF MNEM BST OPERANDS LABEL, 1

STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX

HW (HW(IAR.0-7/INST.8-14)) += R7, BR TO HW(IAR.0-7/INST.8-14)+2

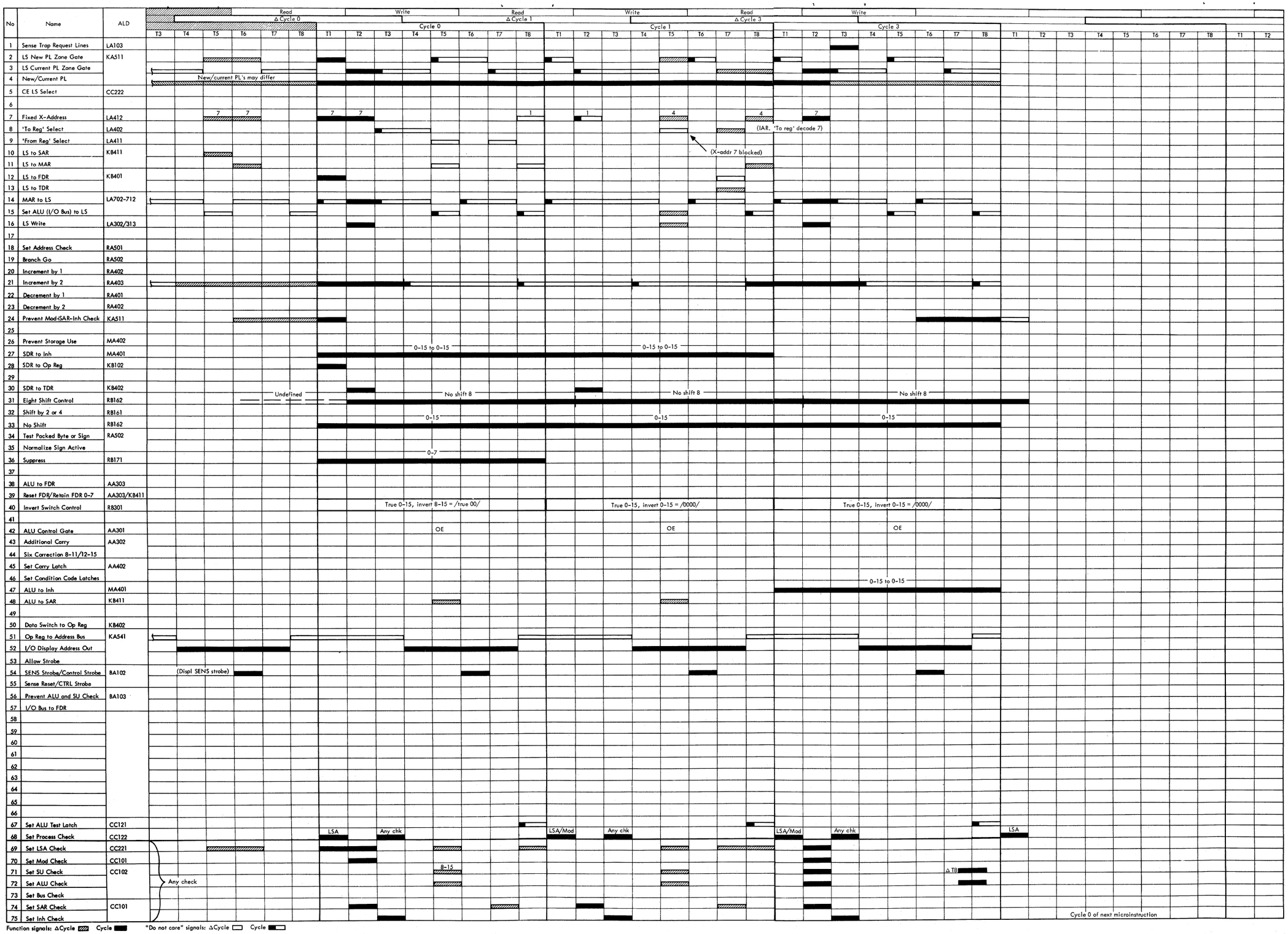
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

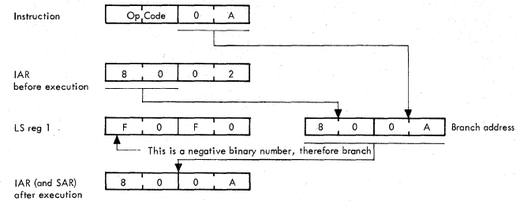
No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59		
60		
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



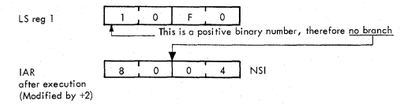
Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▭

The 'to reg' is tested for being zero, minus, plus (not zero), or an invalid address (outside customer area). Successful testing causes a branch. The branch address is a combination of the current block address and the displacement address (low-order byte). If no branch, the updated microinstruction address is used.

Example 1: Successful BM



Example 2: Unsuccessful BM



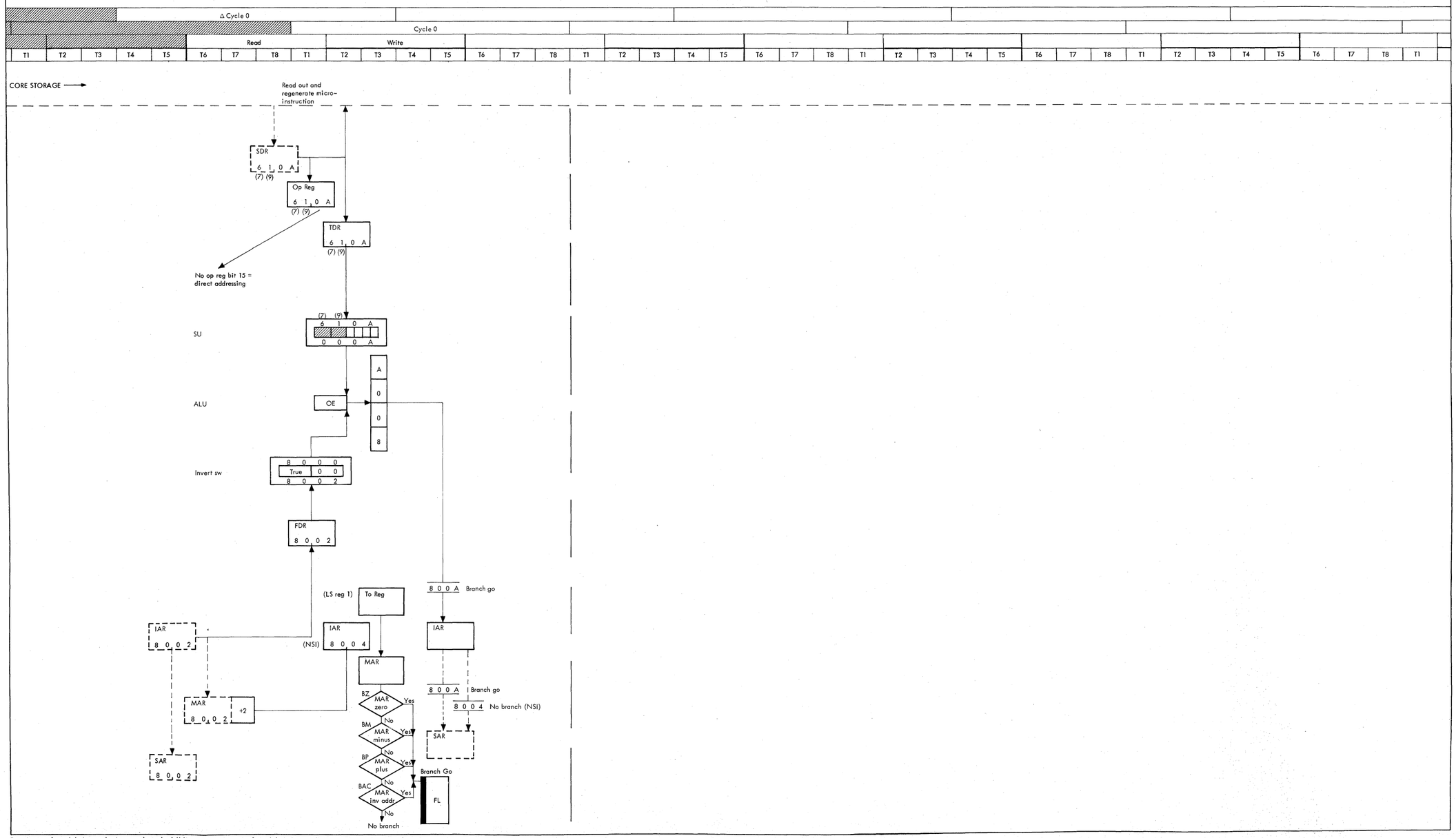
Microinstruction Layout

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
Op Code					To Reg			Displacement Addr								
6					0										0	BZ
6					1										0	BM
7					0										0	BP
7					1										0	BAC

Direct addressing

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
610A	BZ	1,LABEL	BR TO IAR.0-7/INST.8-14 IF R1=0
690A	BM	1,LABEL	BR TO IAR.0-7/INST.8-14 IF R1,LT,0
710A	BP	1,LABEL	BR TO IAR.0-7/INST.8-14 IF R1,GT,0
790A	BAC	1,LABEL	BR TO IAR.0-7/INST.8-14 IF R1 INVALID

Mnemonic
BZ
BM
BP
BAC
Format
RD
Type
Direct Addressing



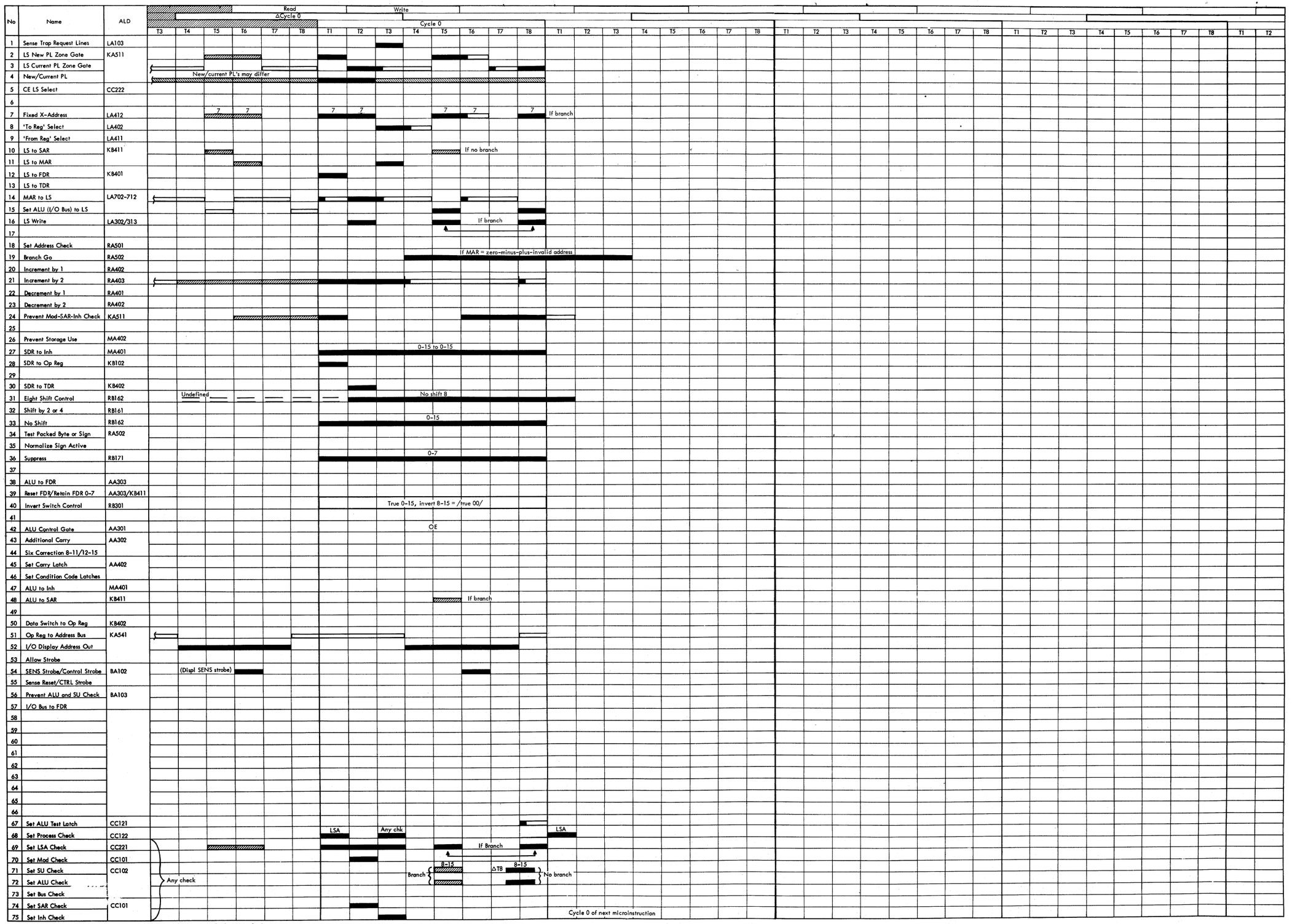
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle

Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

Diagram 5-18. Branch on Binary Zero-Minus-Plus, Address Check (Direct Addressing) (Part 1 of 2) (03723) 2020 ≧ 50,000 FEMDM Vol 2 (8/69)

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59		
60		
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



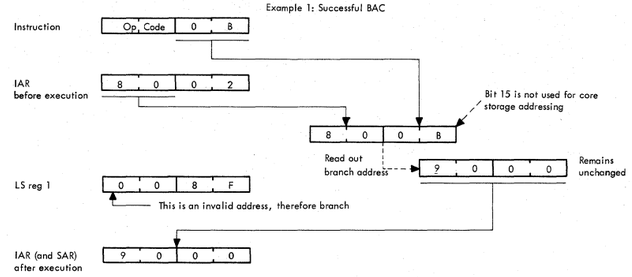
Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▬

● Diagram 5-18. Branch on Binary Zero-Minus-Plus, Address Check (Direct Addressing) (Part 2 of 2) (03723A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

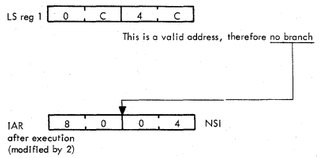
The 'to reg' is tested for being zero, minus, plus (not zero), or an invalid address (outside customer area).

Successful testing causes a branch. The branch address is read out by an address comprising a combination of the current block address and the displacement address (low-order byte). If no branch the update microinstruction address is used.

Example 1: Successful BAC



Example 2: Unsuccessful BAC



Microinstruction Layout

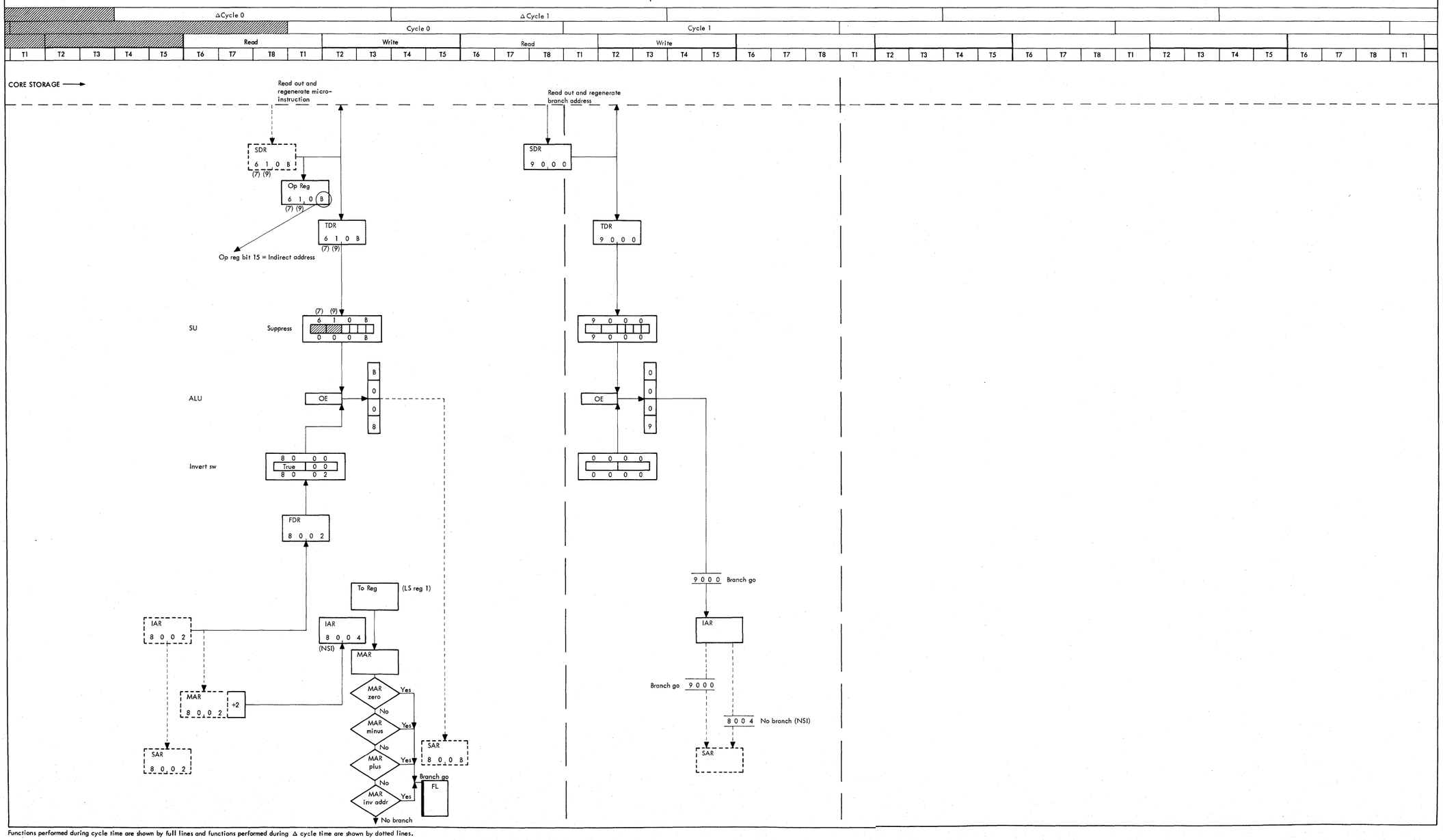
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
Op Code					To Reg			Displacement Addr								Mnemonic
6				0											1	BZ
6				1											1	BM
7				0											1	BP
7				1											1	BAC

Indirect addressing

```
INST    MNEM   OPERANDS          STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
610B    BZ     1,LABEL,I         BR TO HW (IAR.0-7/INST.8-14) IF R1=0
690B    BM     1,LABEL,I         BR TO HW (IAR.0-7/INST.8-14) IF R1,LT,0
710B    BP     1,LABEL,I         BR TO HW (IAR.0-7/INST.8-14) IF R1,GT,0
790B    BAC    1,LABEL,I         BR TO HW (IAR.0-7/INST.8-14) IF R1 INVALID
```

Format: RD

Type: Indirect Addressing

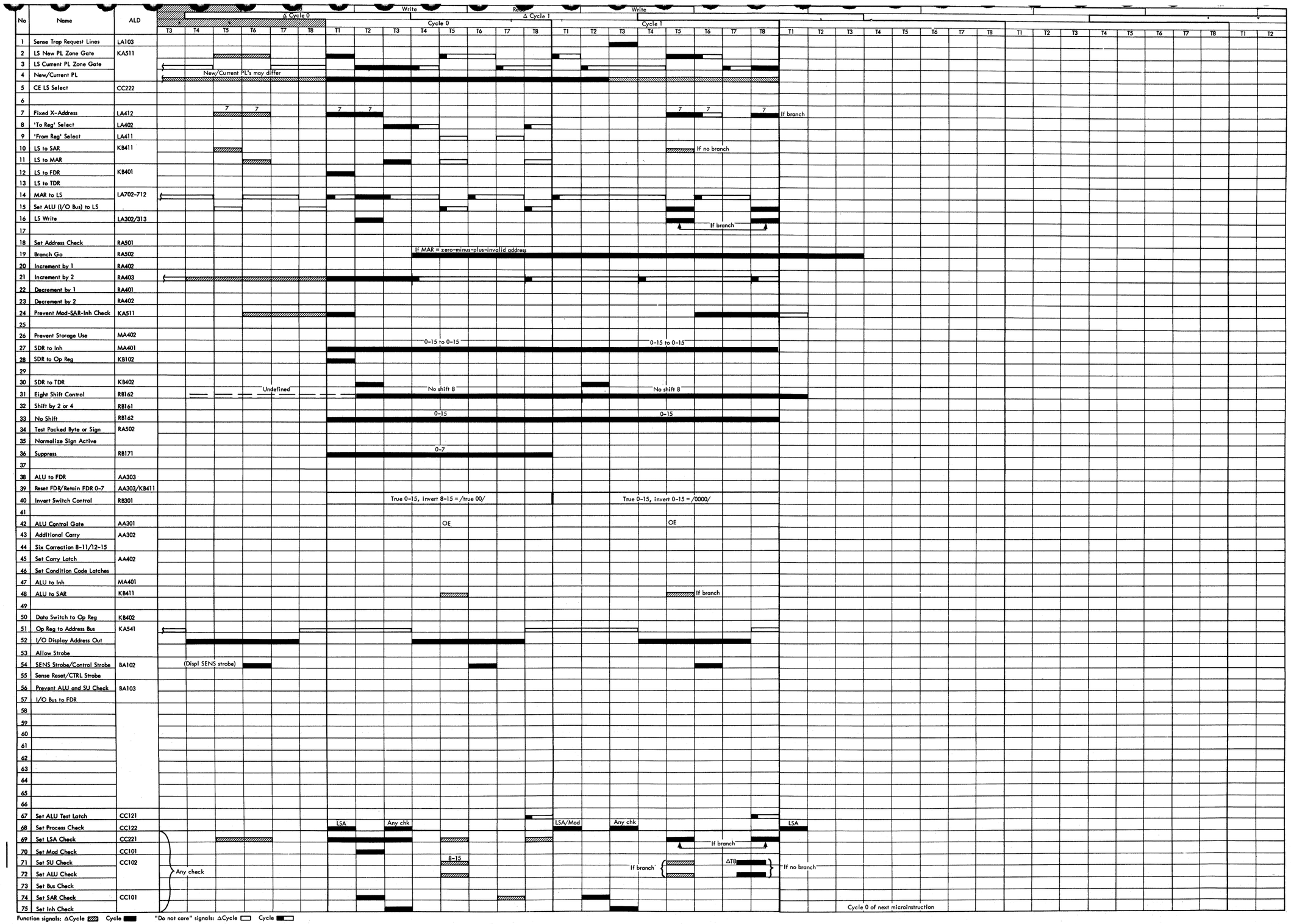


Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle

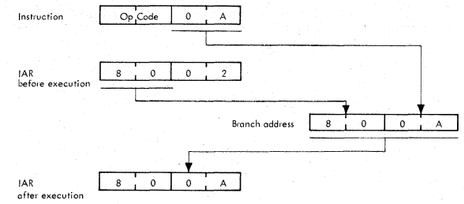
No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59		
60		
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▭

● Diagram 5-19. Branch on Binary Zero-Minus-Plus, Address Check (Indirect Addressing) (Part 2 of 2) (03724A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

An unconditional branch is performed. The branch address is a combination of the current block address and the displacement address (low-order byte).



Microinstruction Layout

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Op Code								Displacement Addr							
8		0	0	0	0										0
To Reg															

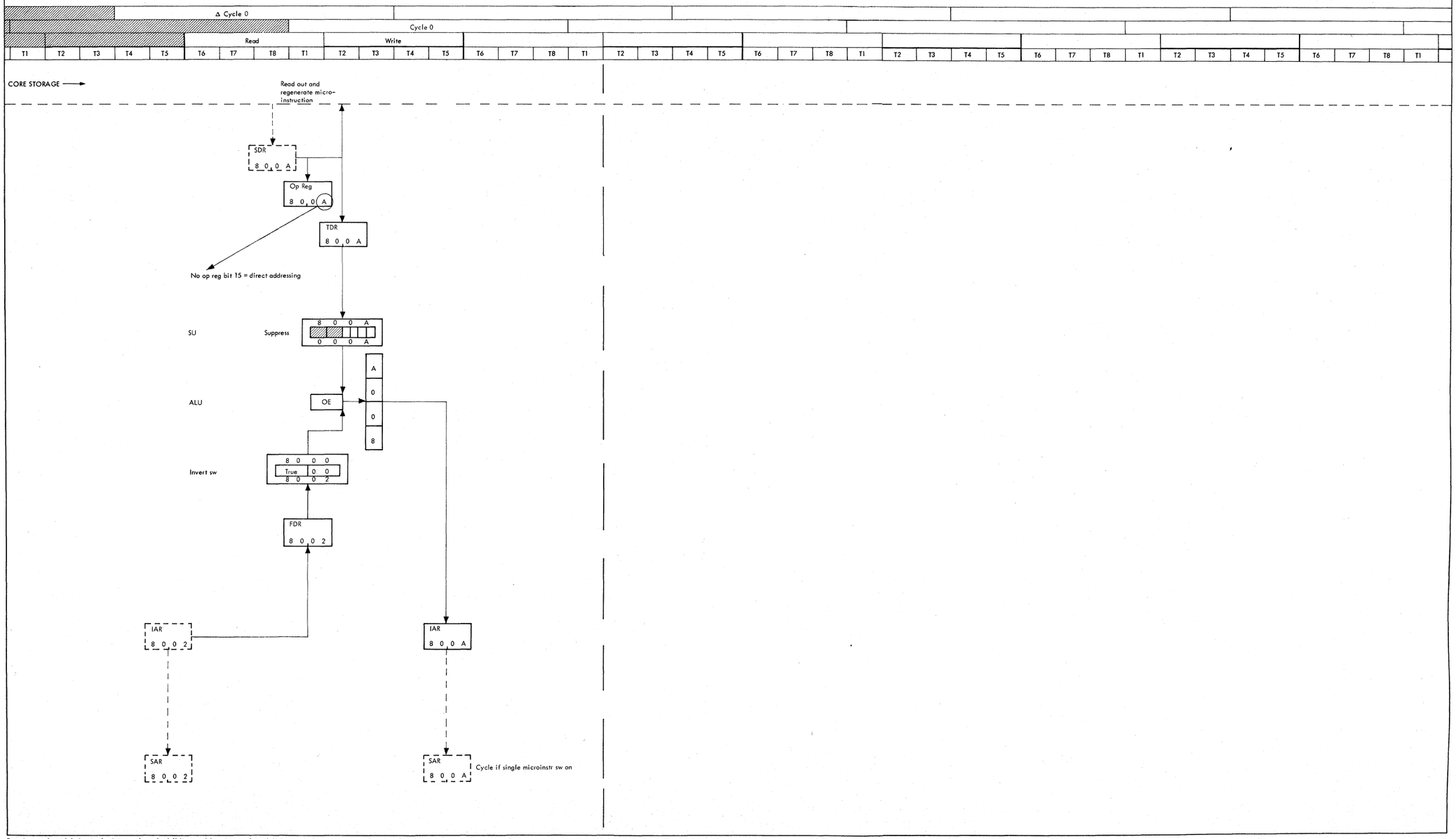
Direct Addressing

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
800A	B	LABEL	BR TO IAR.0-7/INST.8-14

Mnemonic
B
Format
RD
Type
Direct Addressing

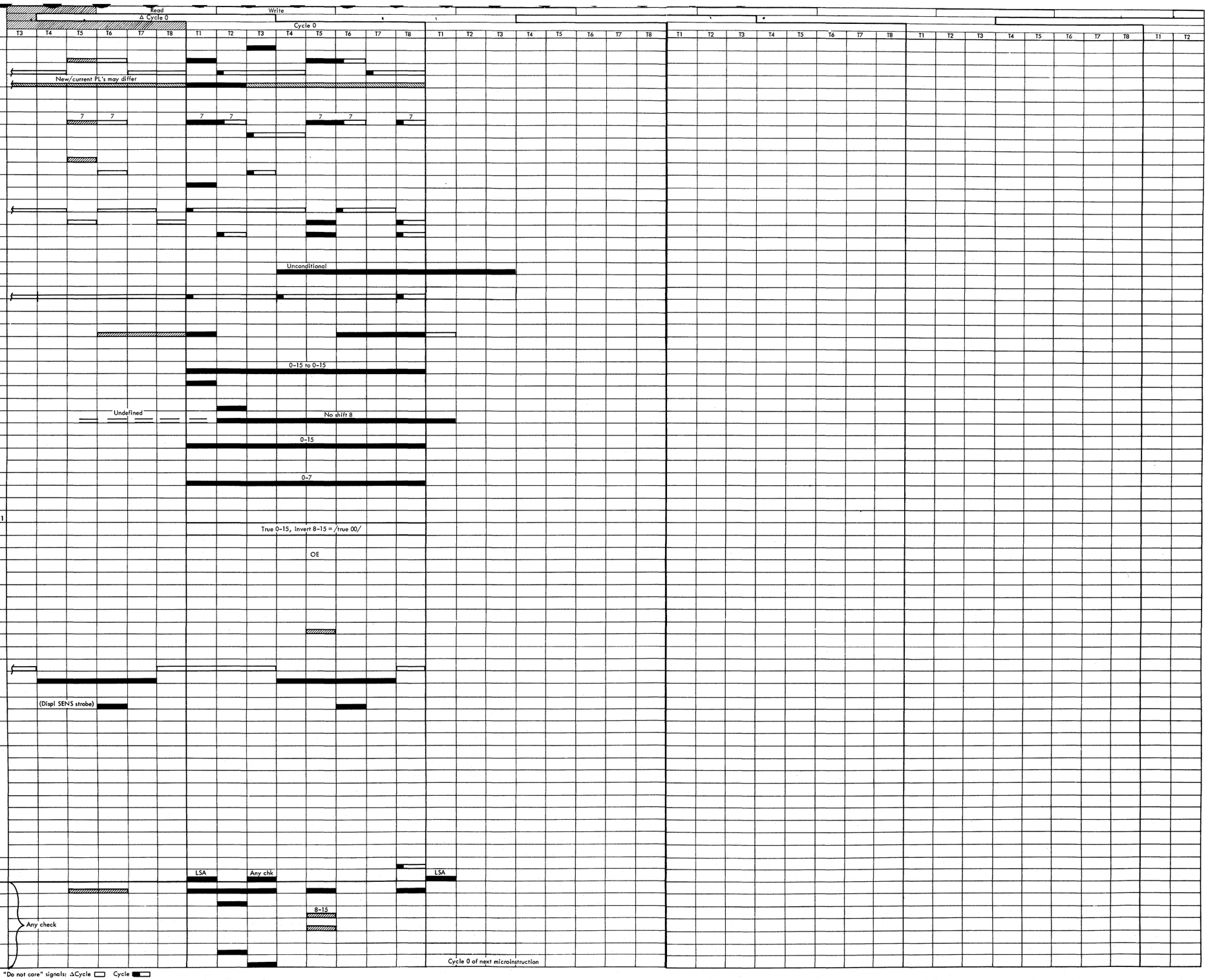
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

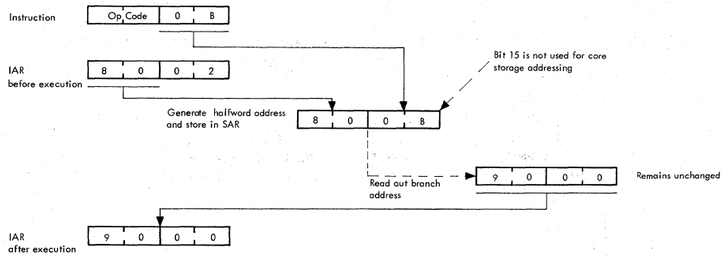
No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59		
60		
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	

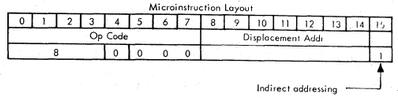


Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▬

● Diagram 5-20. Branch Unconditional (Direct Addressing) (Part 2 of 2) (03725A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

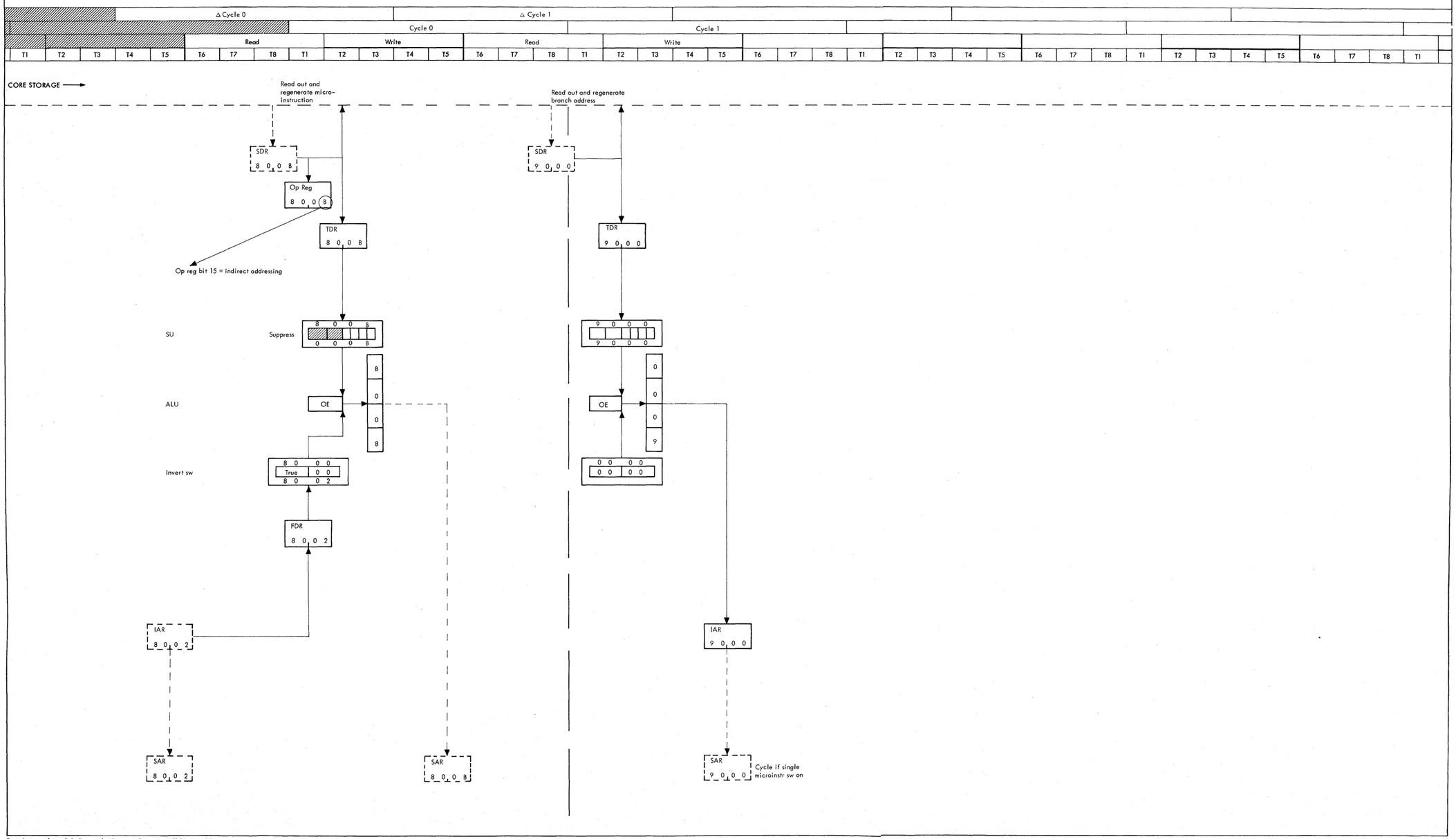
An unconditional branch is performed. The branch address is read out by an address comprising a combination of the current block address and the displacement address (low-order byte)





Mnemonic
B
Format
RD
Type
Indirect Addressing

INST 800B MNEM B OPERANDS LABEL,I STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX BR TO HW (IAR, 0-7/INST, 8-14)

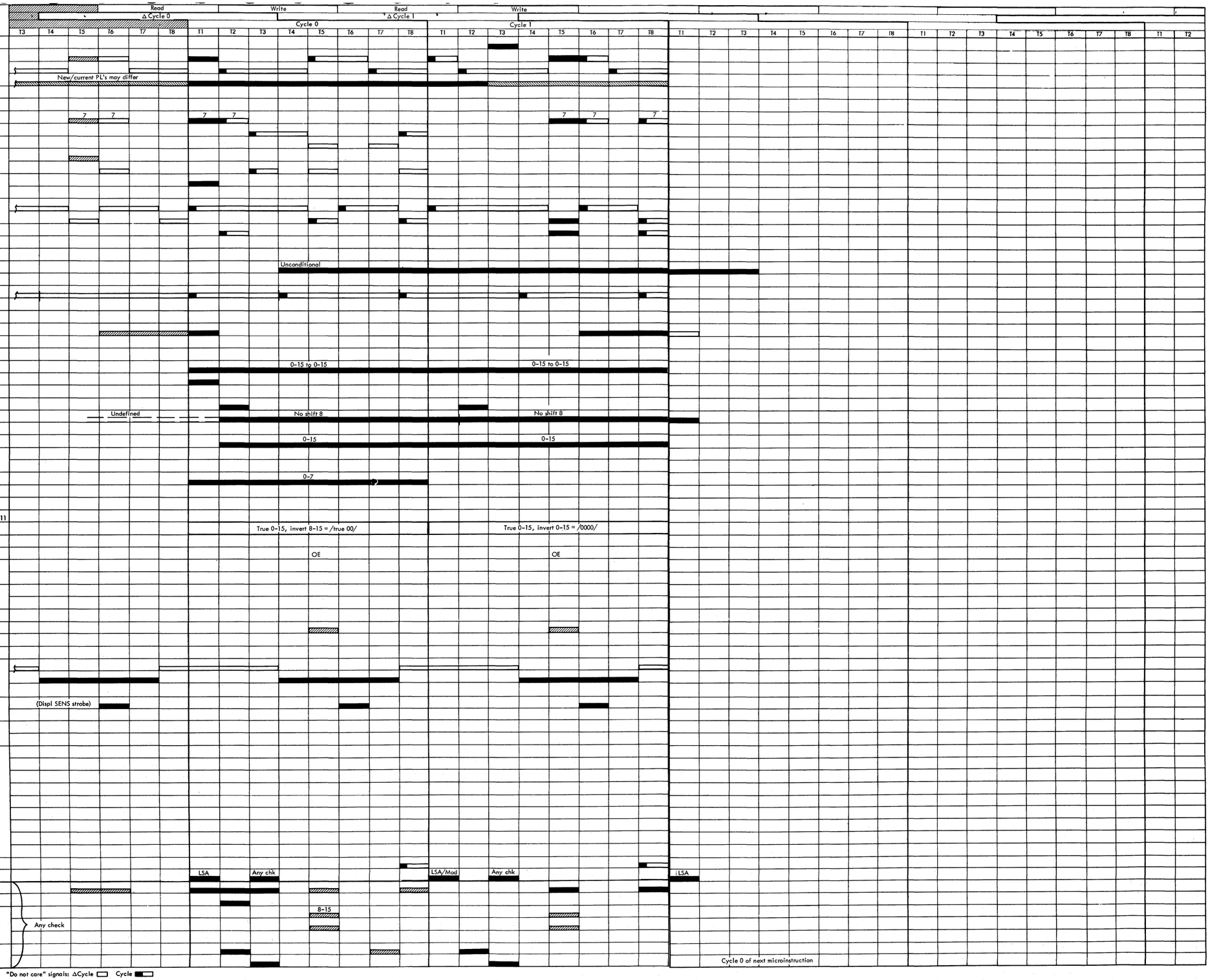


Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle

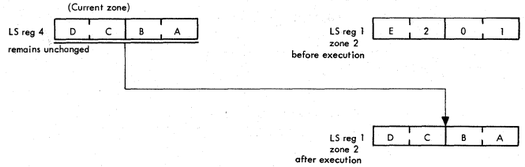
Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59		
60		
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▬

LS register 4 of the current LS zone (defined by the current program level) is stored into the 'from reg' of the LS zone specified in the 'to reg' field.



Microinstruction Layout

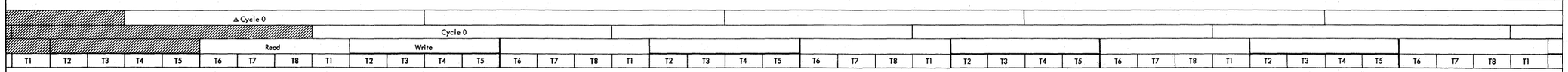
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Op Code								To Reg				From Reg			
8		0	0	1	0	0				Zone		0			

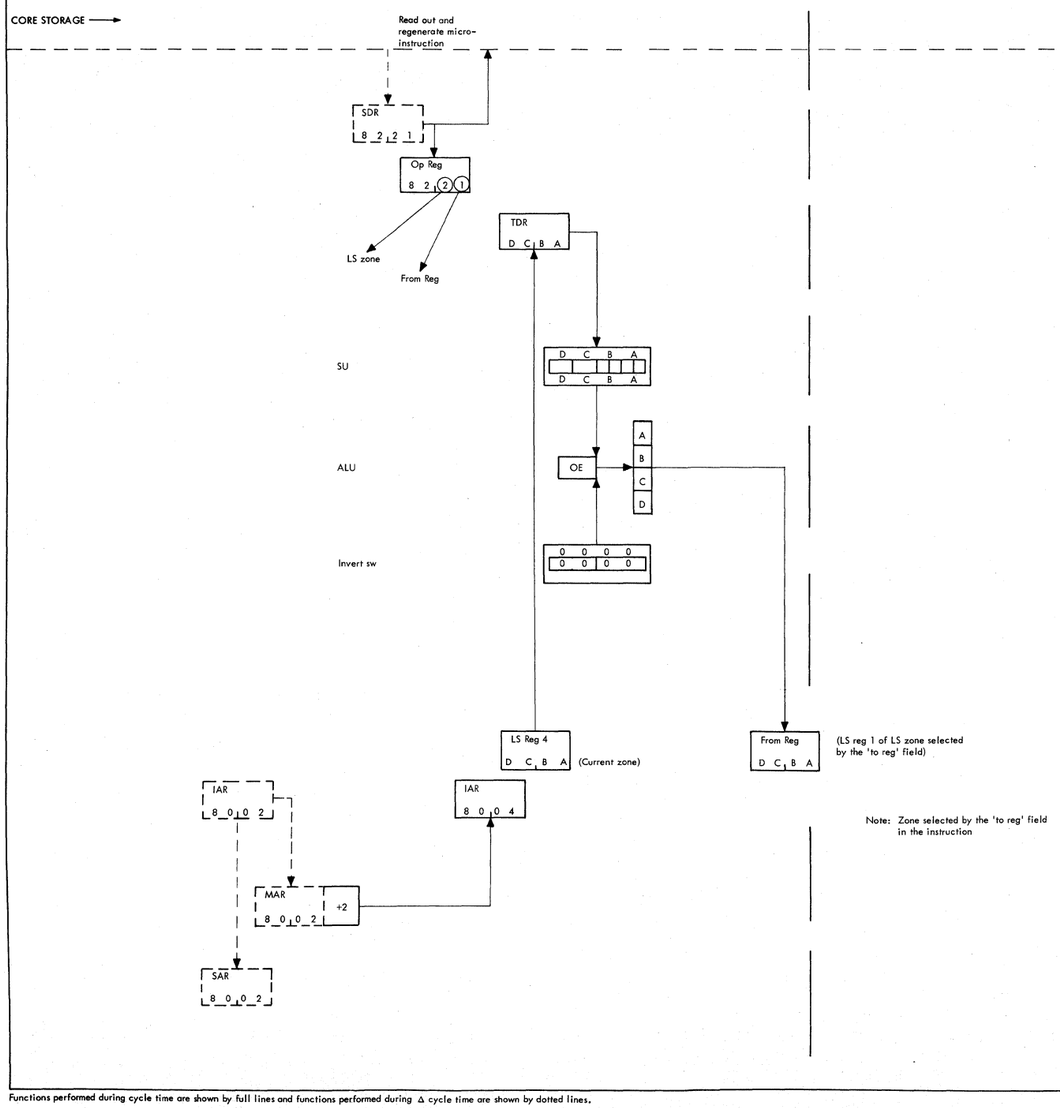
Mnemonic
STR
Format
FF
Type

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
8221	STR	2,1	R1 PL2*=R4

Note: For "Do not care" functions refer to timing chart below.

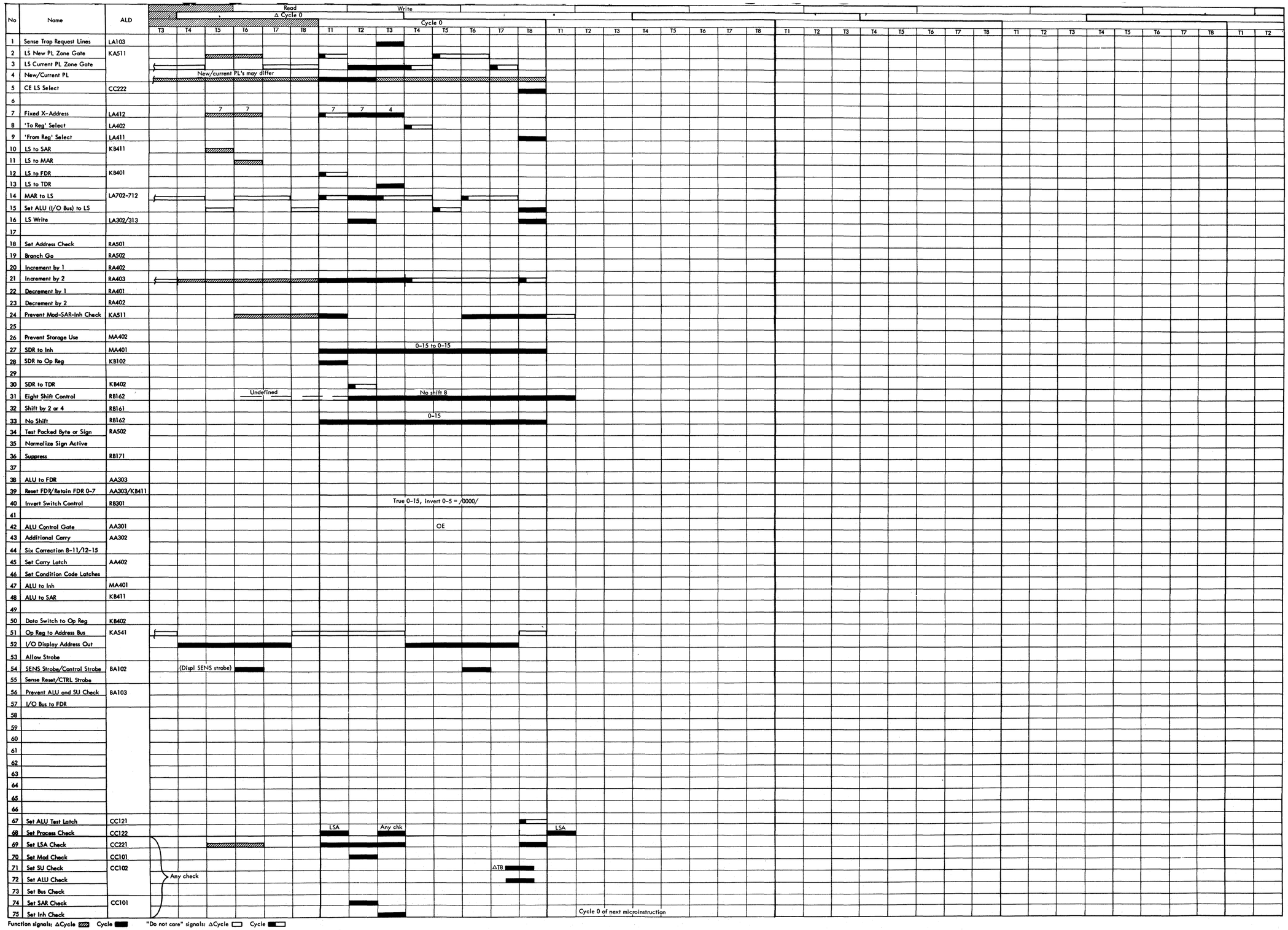
"Do not care" signals:
- ΔCycle
- Cycle





Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

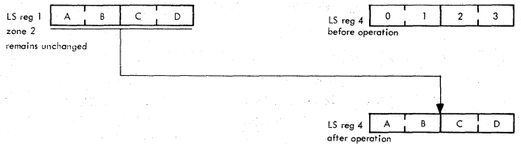
No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59		
60		
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▬

Diagram 5-22. Store Zone Register (Part 2 of 2) (03727A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

The 'to reg' field specifies an LS zone (0 to 7), the 'from reg' of which is loaded into LS register 4 of the current LS zone (defined by the current program level (PL)').

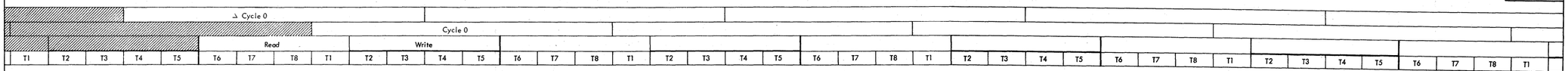


Microinstruction Layout

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Op Code									To Reg			From Reg			
8	0	0	1	1	0	Zone						0			

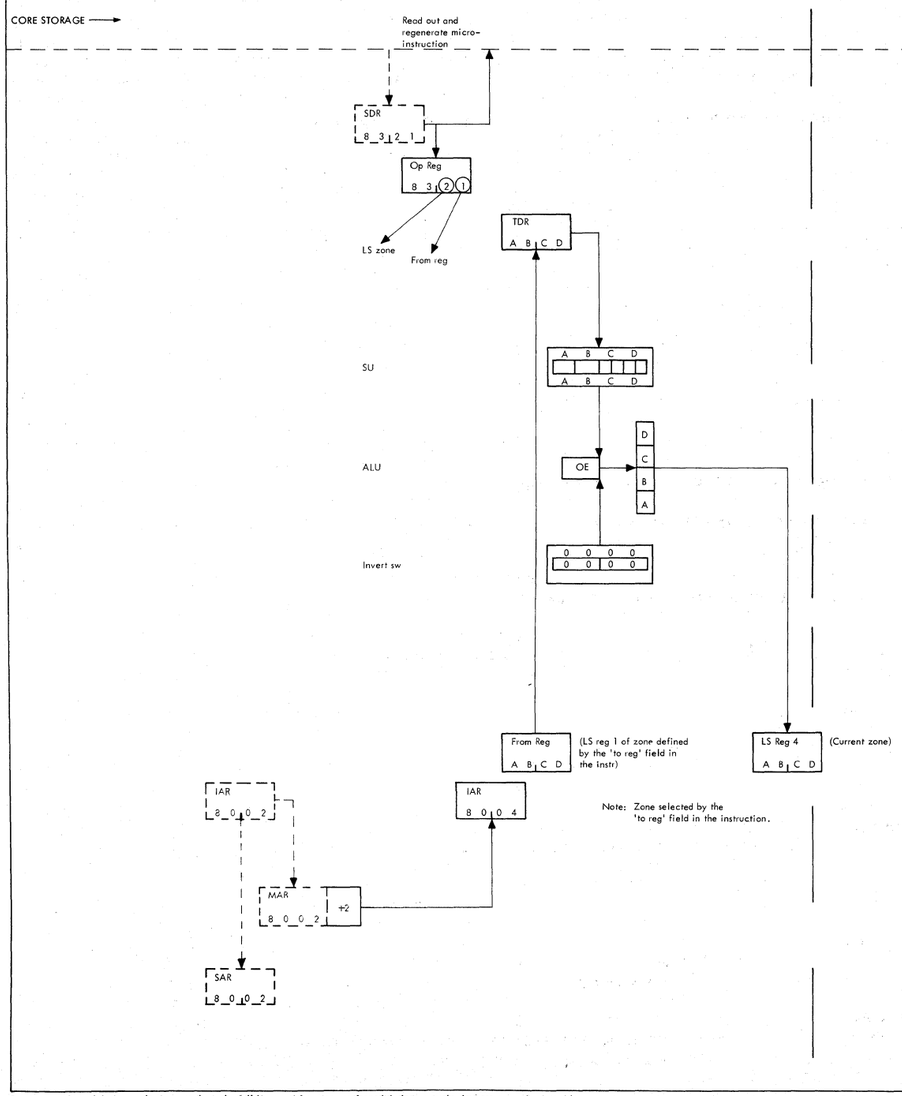
INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
8321	LR	2,1	R4+=R1 PL2

Mnemonic
LR
Format
FF
Type



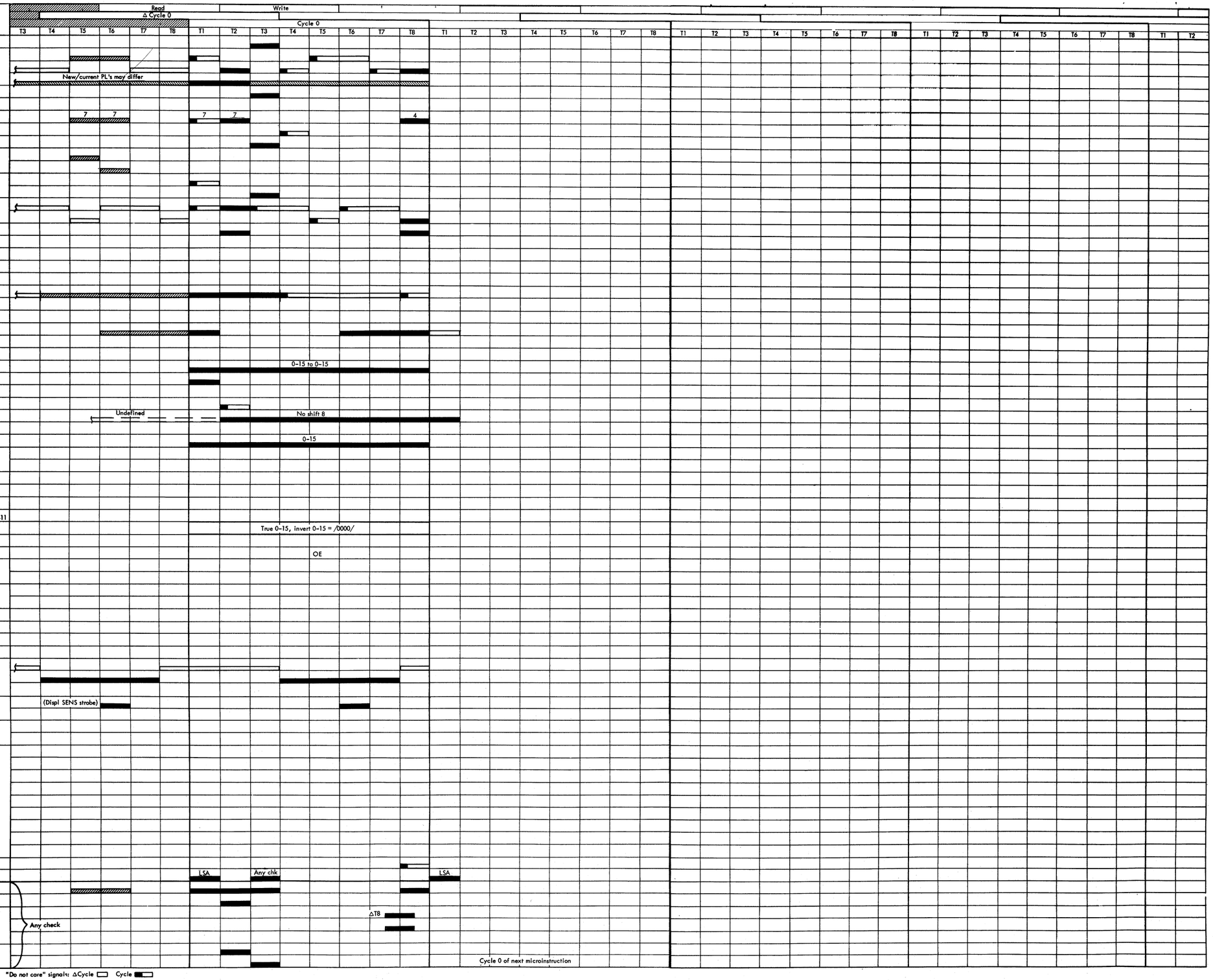
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
- ΔCycle
- Cycle



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59		
60		
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	

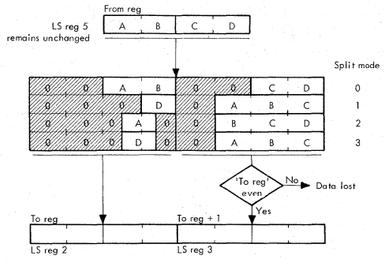


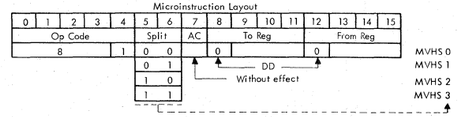
Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▭

Diagram 5-23. Load Zone Register (Part 2 of 2) (03728A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

The 'from reg' is split according to the selected split mode (0 to 3). The result of the split is set into the 'to reg' and the next highest LS register ('to reg' + 1). The 'to reg' must be an even numbered register (but not 6) otherwise the data to be placed into the next highest LS register will be lost.

Address check is ignored. The 'from reg' remains unchanged. 'From reg' and 'to reg' may be the same LS register.



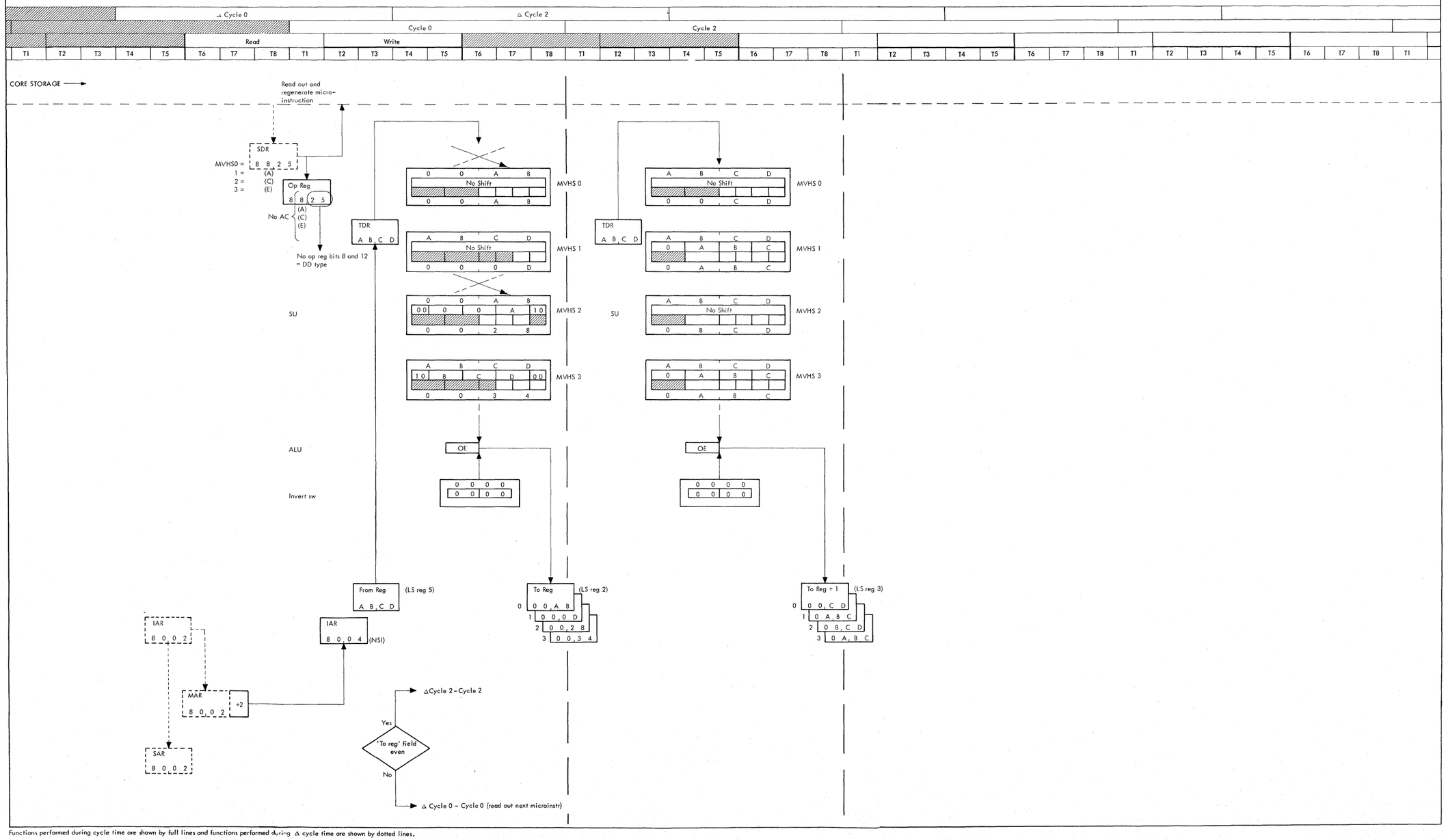


Mnemonic
MVHS
Format
FF
Type
DD

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
8825	MVHS	2,5,0	R2+='00'/R5.0-7,R3 ='00'/R5.8-15
8A25	MVHS	2,5,1	R2+='000'/R5.12-15,R3 ='0'/R5.0-11
8C25	MVHS	2,5,2	R2+=SL 2 '000'/R5.0-3, R3 ='0'/R5.4-15
8E25	MVHS	2,5,3	R2+=SL 2 '000'/R5.12-15, R3 ='0'/R5.0-11

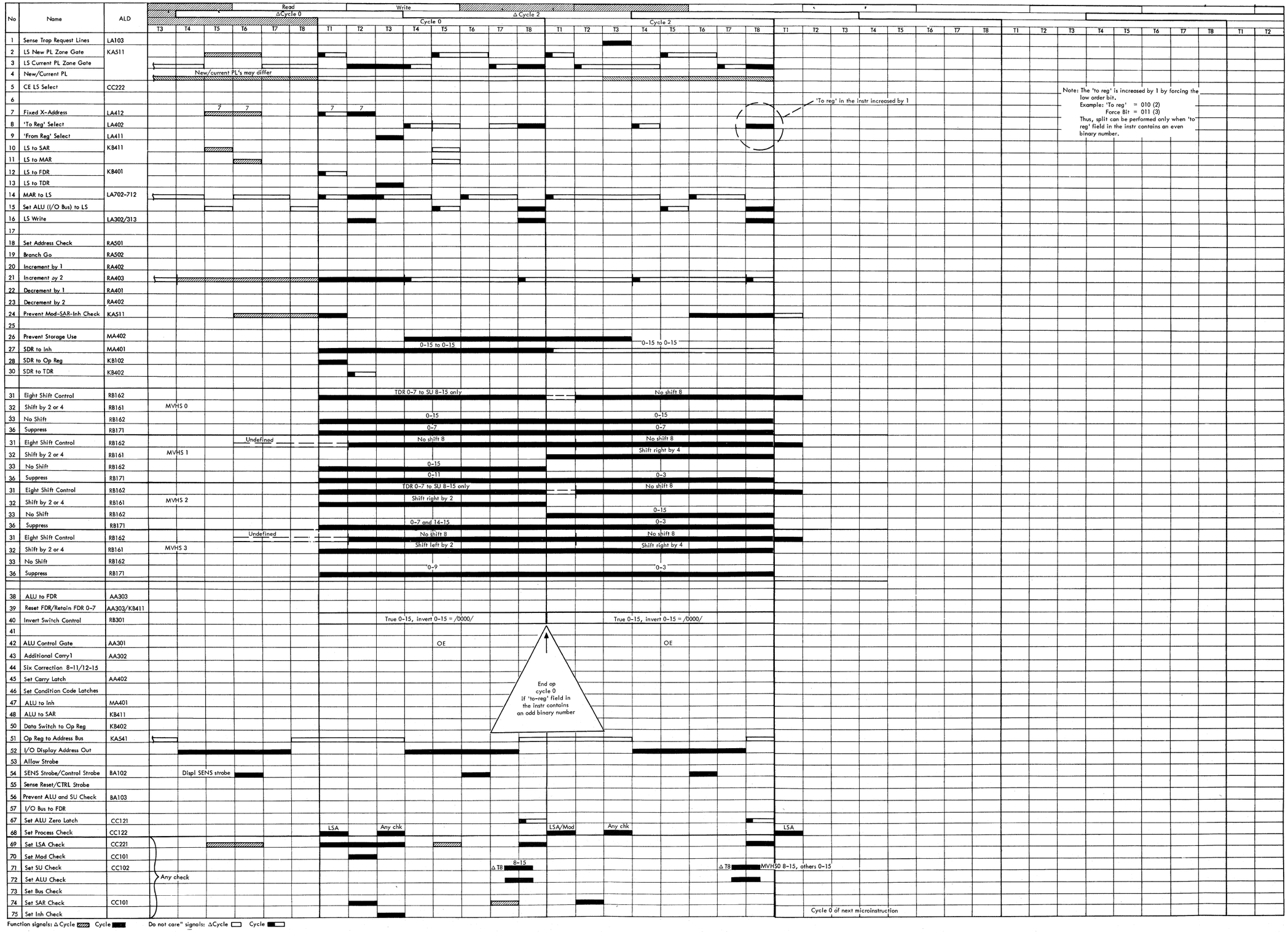
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
△Cycle
Cycle



Functions performed during cycle time are shown by full lines and functions performed during △ cycle time are shown by dotted lines.

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
36	Suppress	RB171
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
36	Suppress	RB171
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
36	Suppress	RB171
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry1	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
67	Set ALU Zero Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	

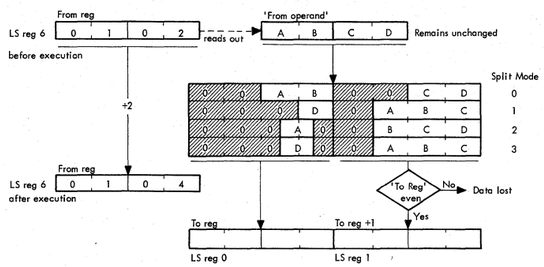


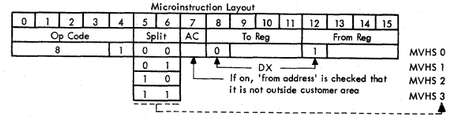
● Diagram 5-24. Move Halfword and Split (DD) (Part 2 of 2) (03729A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

The halfword read out by the 'from reg' is split according to the selected split mode (0-3). The result of the split is set into 'to reg' and the next higher LS register ('to reg' + 1). The 'to reg' must be an even numbered register (but not 6) otherwise the data to be placed into the next higher LS register is lost

If the AC bit (instruction bit 7) is on, an address check occurs when the 'from reg' address is outside customer area. The 'from reg' address is incremented by 2.

The core storage halfword read out by the 'from reg' remains unchanged.



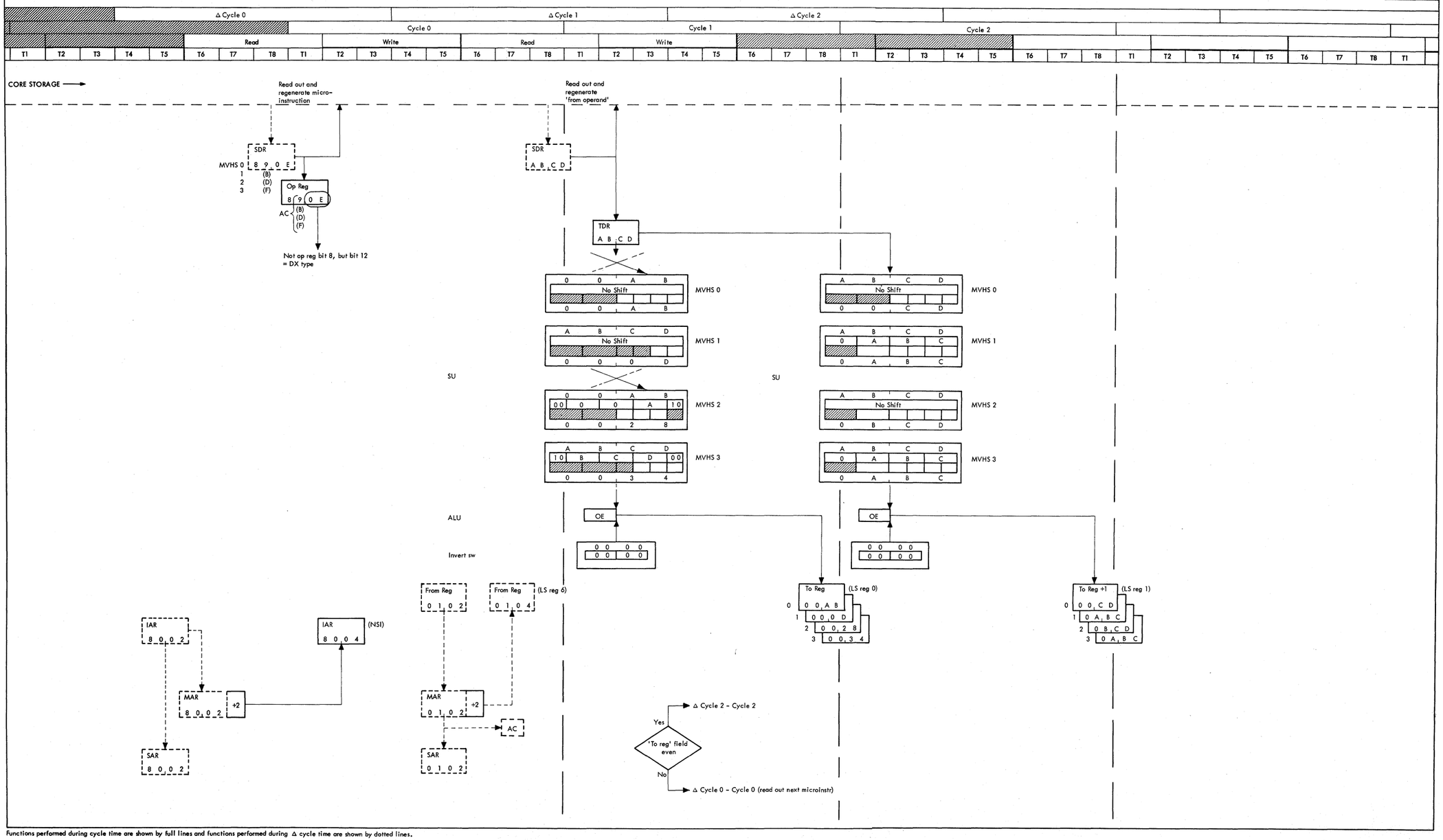


Mnemonic
MVHS
Format
FF
Type
DX

INST	MNEM	OPERANDS	STATEMENT$ AGCORDING TO STANDARD GEB 0-1046-XXX
890E	MVHS	0,6I,0,AC	R0+=#00#/HW(R6,AC). 0-7,R1 =#00#/HW(R6,+2). 8-15
8B0E	MVHS	0,6I,1,AC	R0+=#000#/HW(R6,AC). 12-15, R1 =#0#/HW(R6,+2). 0-11
8D0E	MVHS	0,6I,2,AC	R0+=SL 2 #000#/HW(R6,AC). 0-3,R1 =#0#/HW(R6,+2). 4-15
8F0E	MVHS	0,6I,3,AC	R0+=SL 2 #000#/HW(R6,AC). 12-15,R1 =#0# HW(R6,+2). 0-11

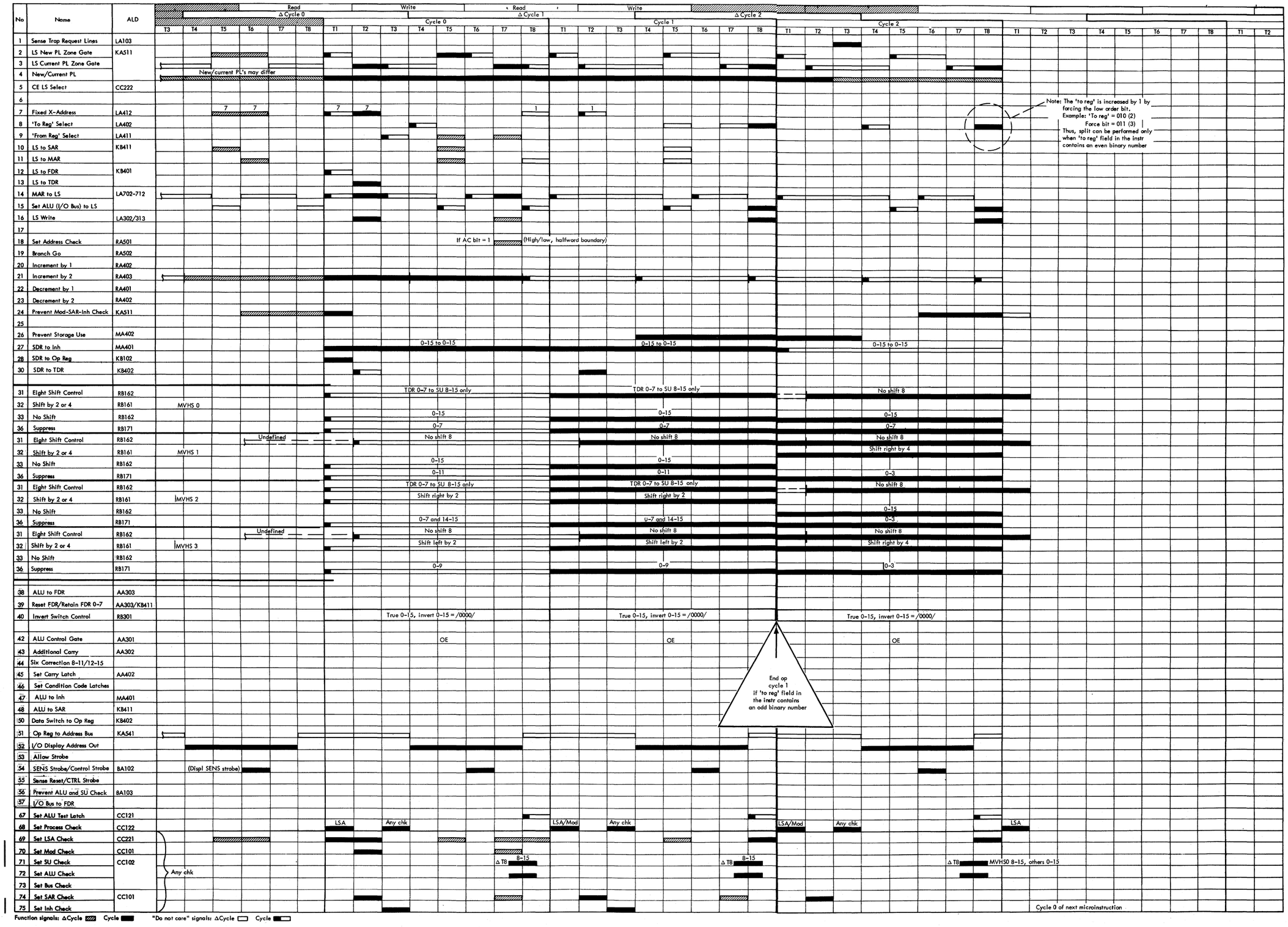
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
36	Suppress	RB171
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
36	Suppress	RB171
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
36	Suppress	RB171
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	

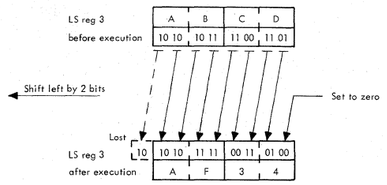


● Diagram 5-25. Move Halfword and Split (DX) (Part 2 of 2) (03730A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

The 'from reg' is shifted left or right as specified in the shift-amount field (bits 5, 6, 7 of the microinstruction). The shift result is set into 'to reg'. The 'from reg' remains unchanged.

'From reg' and 'to reg' may be the same LS register.

Example: Shift left by 2



Microinstruction Layout

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
Op Code					Shift			To Reg				From Reg				
9				0				0				0				SLM
9				1				0				0				SRM

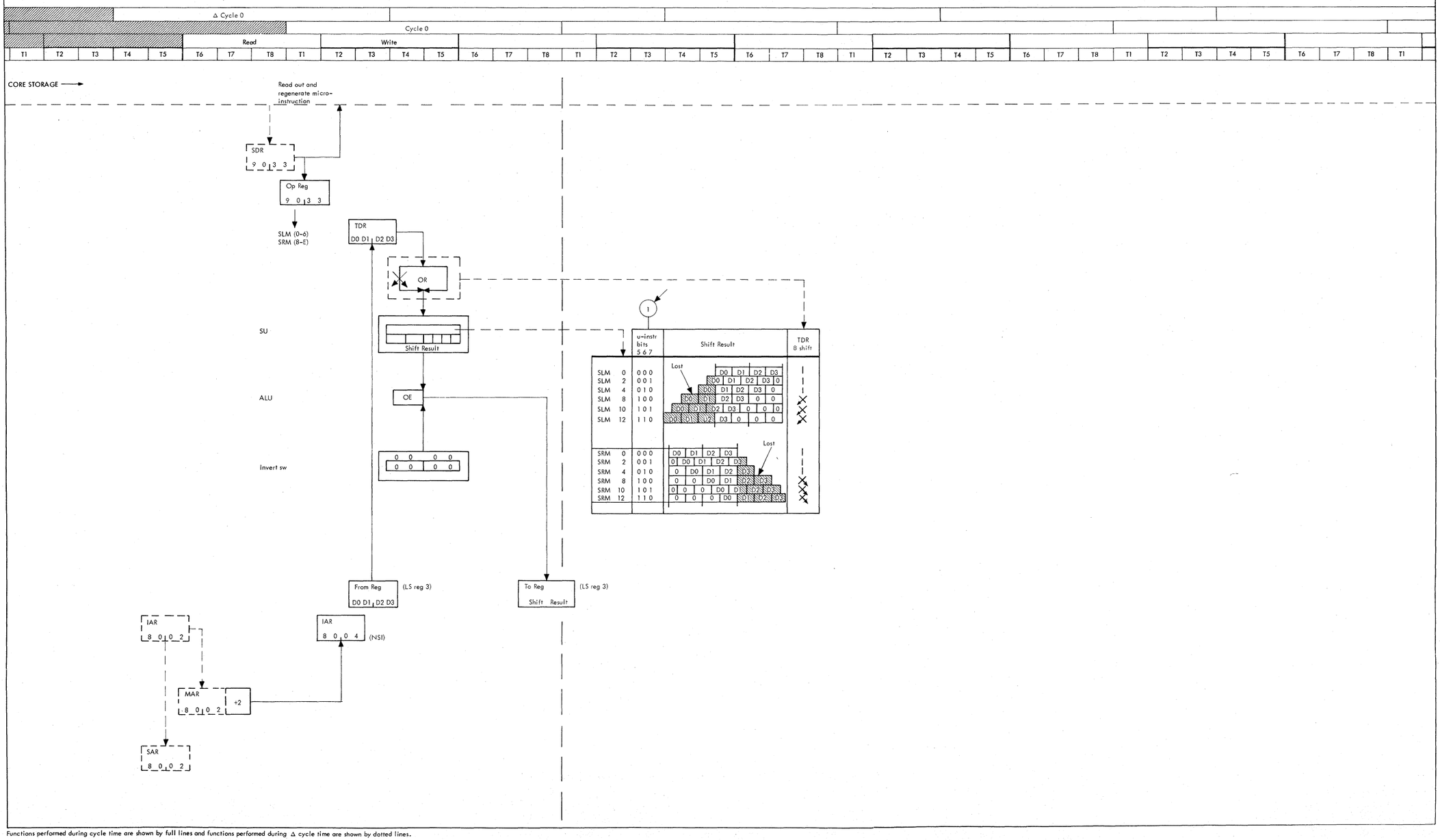
DD

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
9033	SLM	3,3,0	R3+=SL0 R3

Mnemonic
SLM
SRM
Format
FF
Type
DD

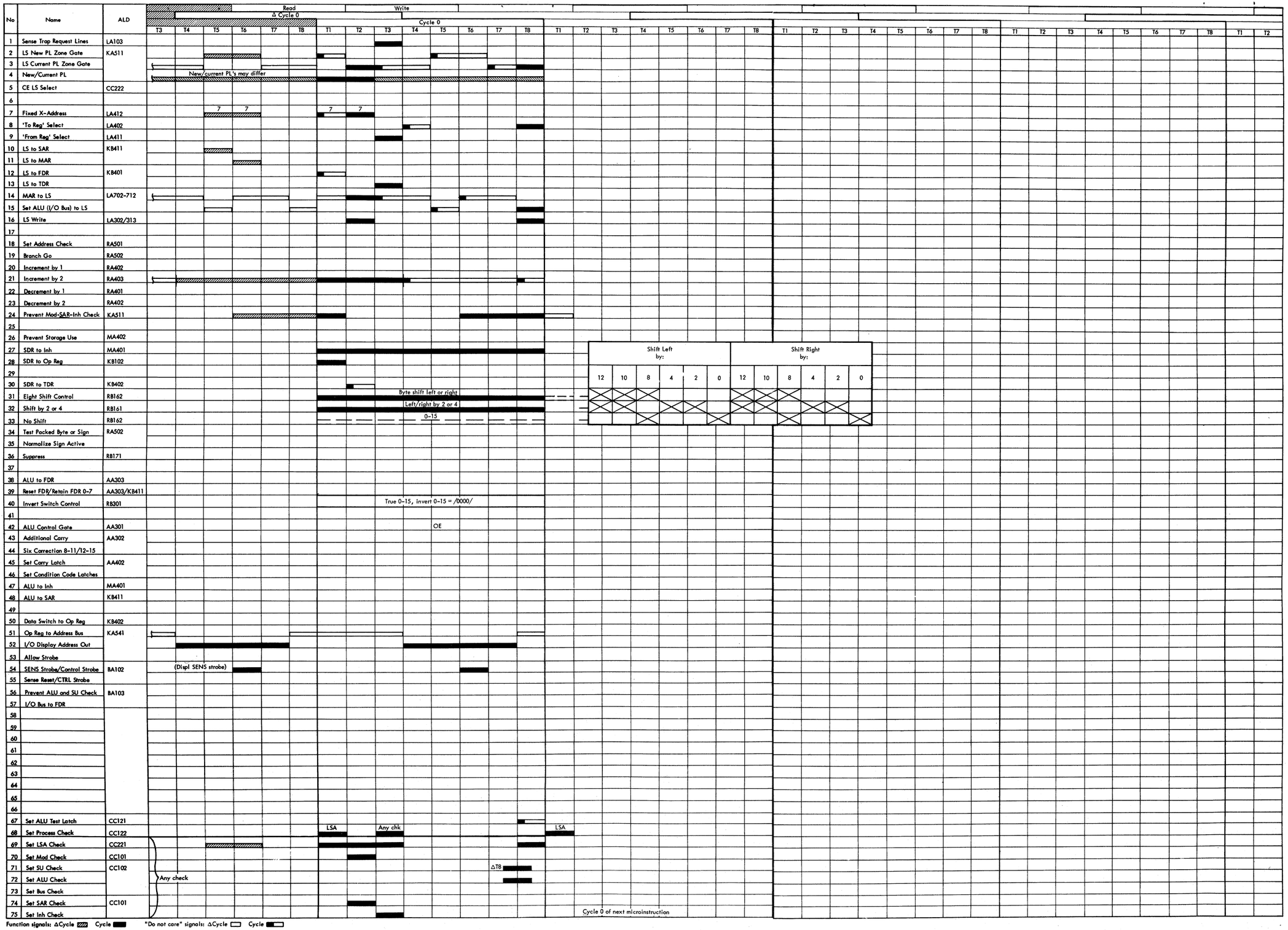
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59		
60		
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle ▭ Cycle ▬

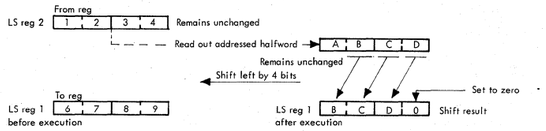
Diagram 5-26. Shift Left/Right and Move (DD) (Part 2 of 2) (03731A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

The halfword read out by the 'from reg' is shifted left or right as specified in the shift-amount field (bits 5, 6, 7 of the microinstruction).

The shift result is set into the 'to reg'.

The core storage halfword read out by the 'from reg' remains unchanged.

Example: Shift left by 4



Microinstruction Layout

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
Op Code				Shift				To Reg				From Reg				
9				0				0				1				SLM
9				1				0				1				SRM

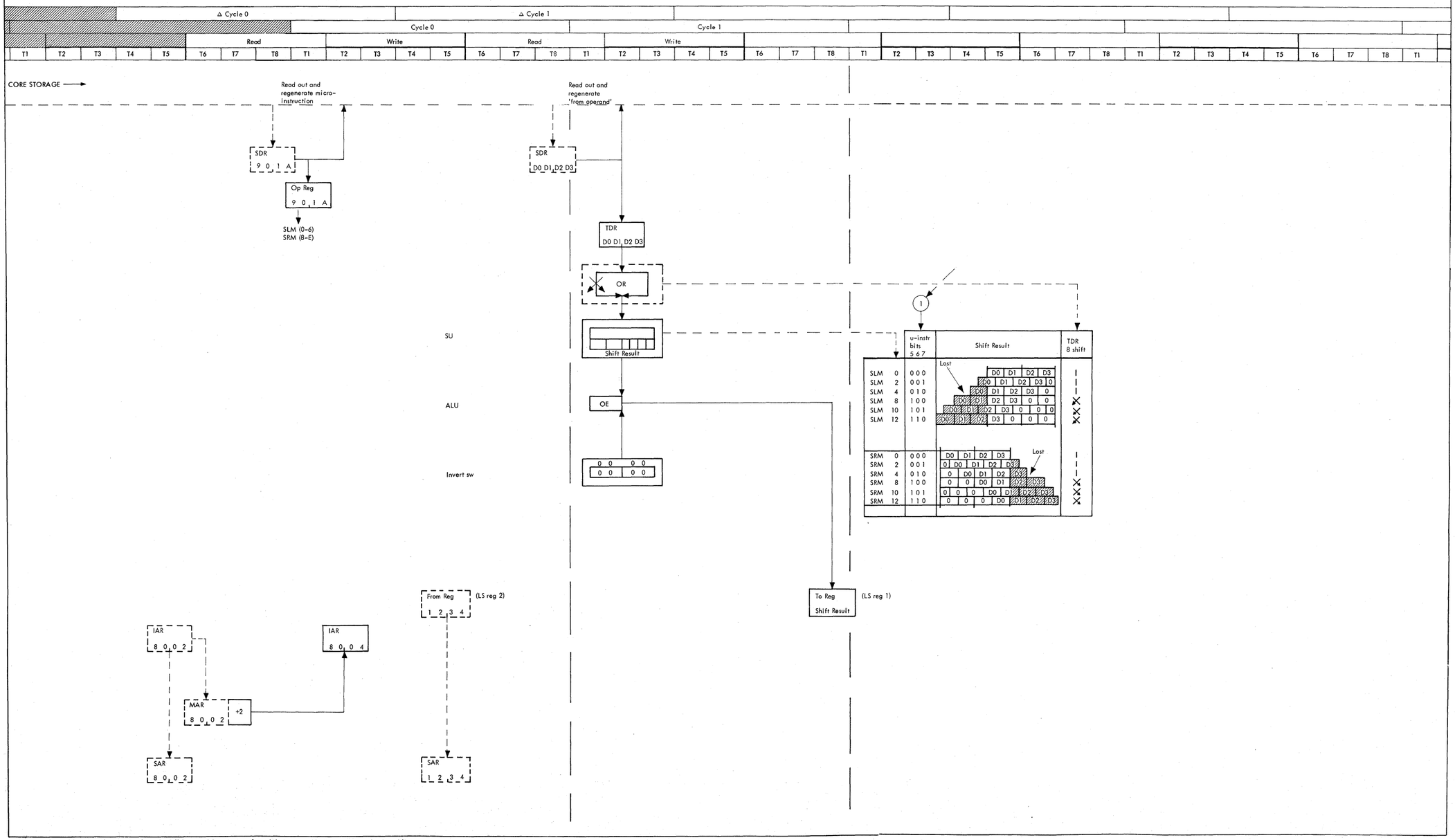
DX

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
901A	SLM	1,21,0	R1←SL0 HW(R2)

Mnemonic
SLM
SRM
Format
FF
Type
DX

Note: For "Do not care" functions refer to timing chart below.

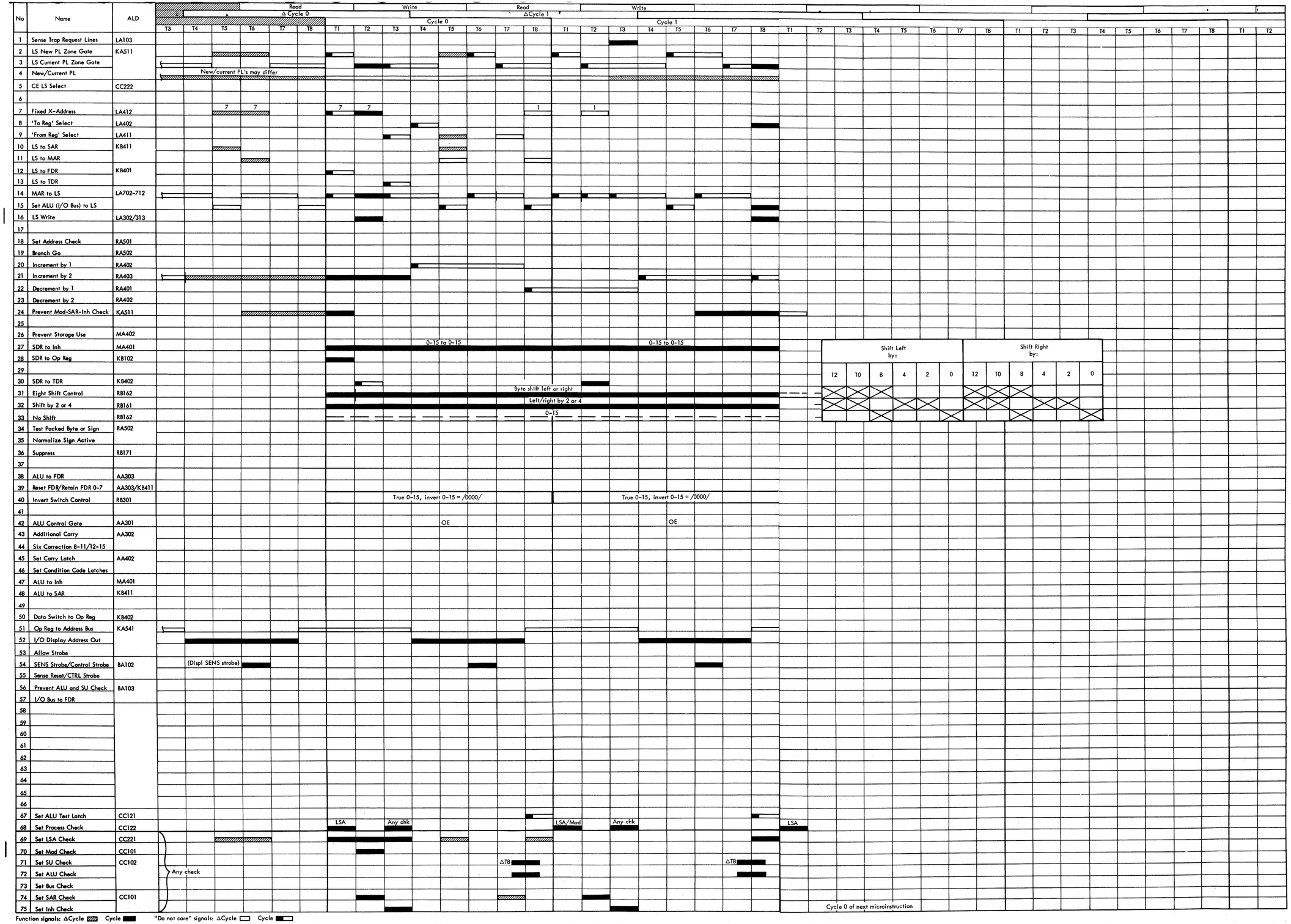
"Do not care" signals:
ΔCycle
Cycle



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

Diagram 5-27. Shift Left/Right and Move (DX) (Part 1 of 2) (03732) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59		
60		
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	

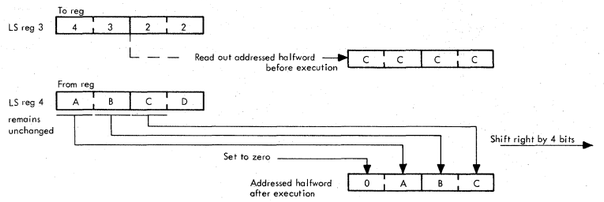


Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ■

● Diagram 5-27. Shift Left/Right and Move (DX) (Part 2 of 2) (03732A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

The 'from reg' is shifted left or right as specified in the shift amount field (bits 5, 6, 7 of the microinstruction). The shift result is stored into the core storage halfword addressed by the 'to reg'. The 'from reg' remains unchanged.

Example: Shift right by 4



Microinstruction Layout

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
Op Code					Shift			To Reg				From Reg				
9				0				1				0				SLM
9				1				1				0				SRM

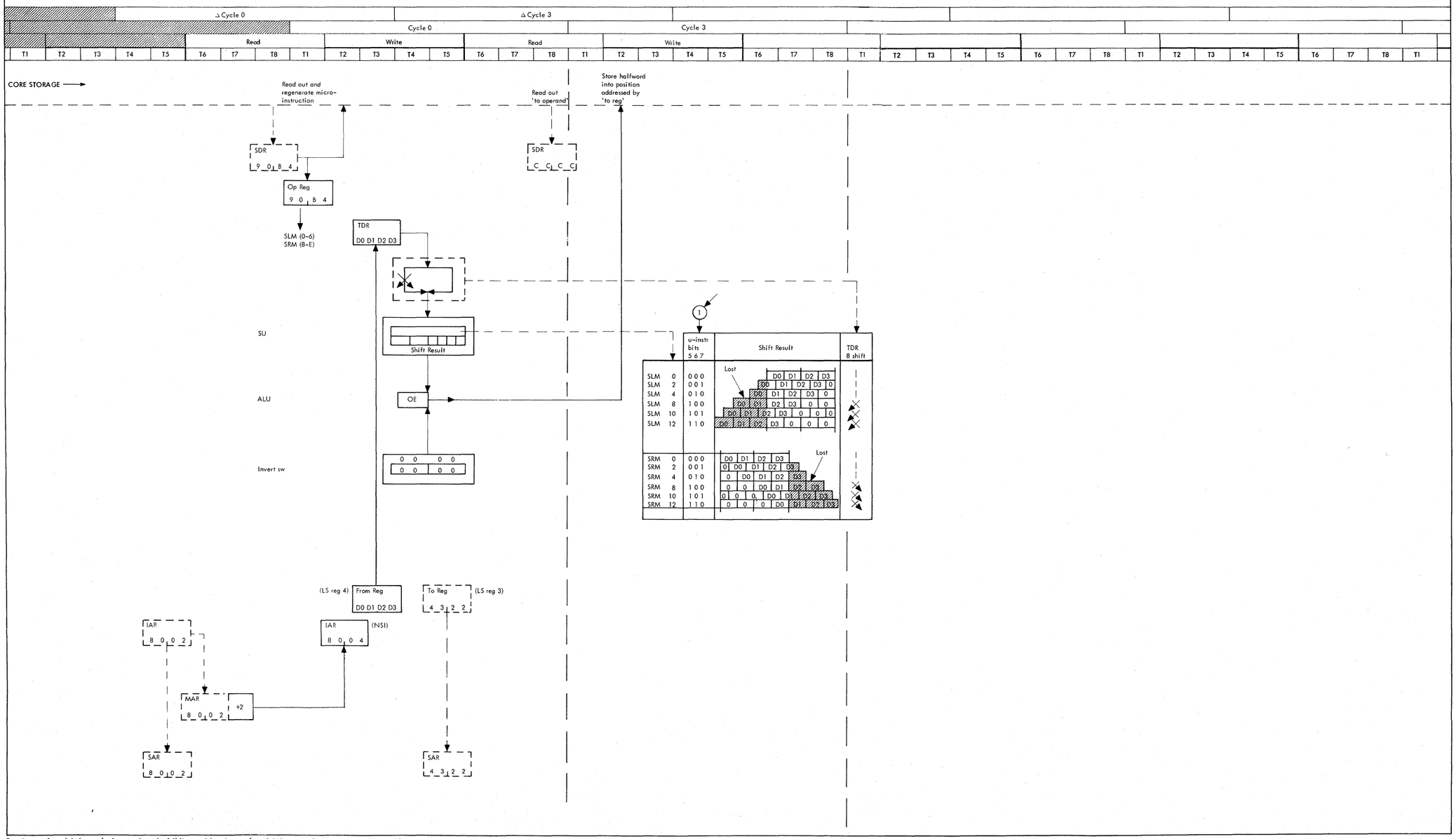
XD

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD C2B 0-1046-XXX
90B4	SLM	3I,4,0	HW(R3)*=SL0 R4

Mnemonic
SLM
SRM
Format
FF
Type
XD

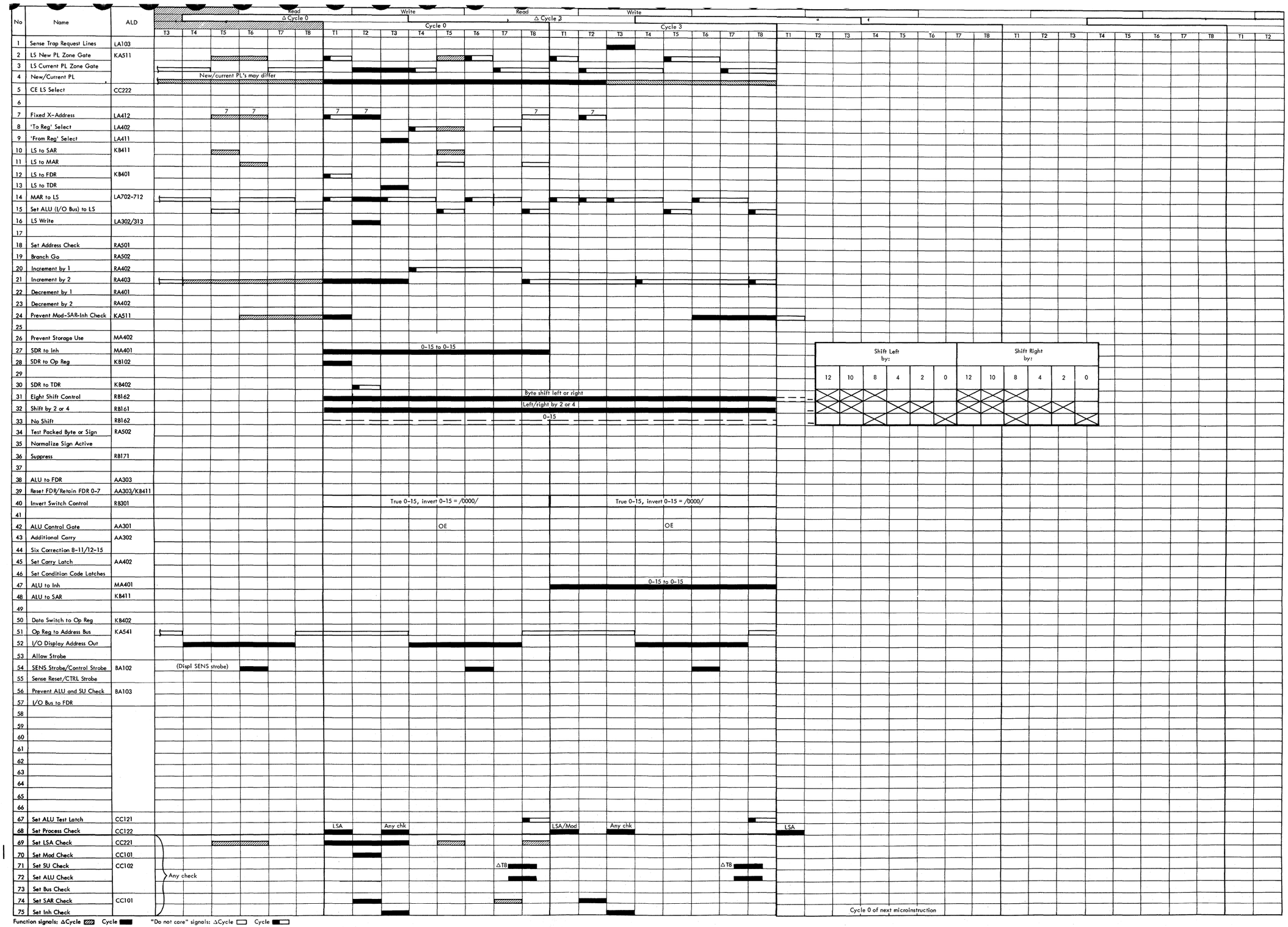
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

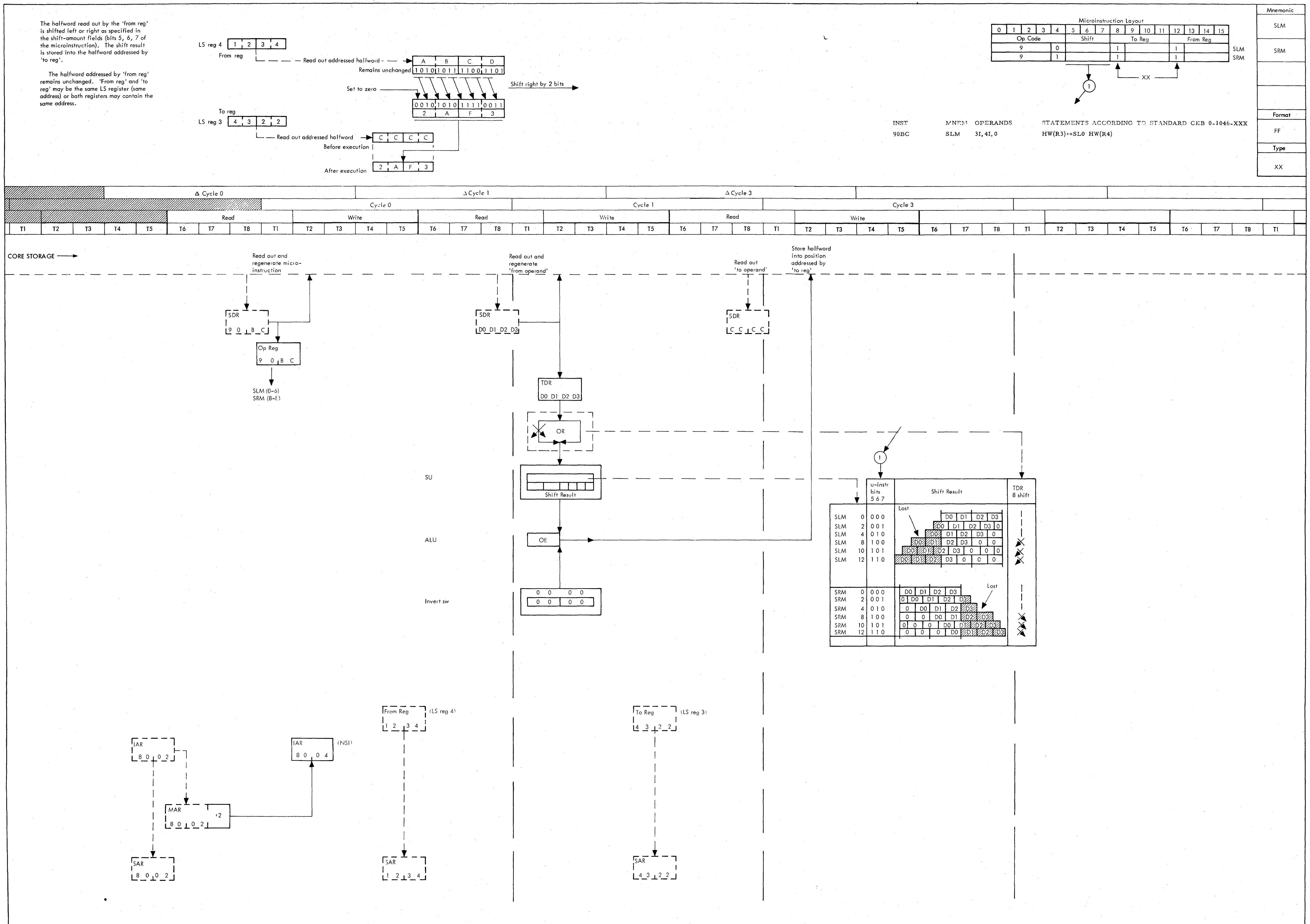
No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59		
60		
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



Shift Left by:						Shift Right by:					
12	10	8	4	2	0	12	10	8	4	2	0
X	X	X				X	X	X			
X	X		X	X		X	X		X	X	
		X			X			X			X

Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▬

● Diagram 5-28. Shift Left/Right and Move (XD) (Part 2 of 2) (03733A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

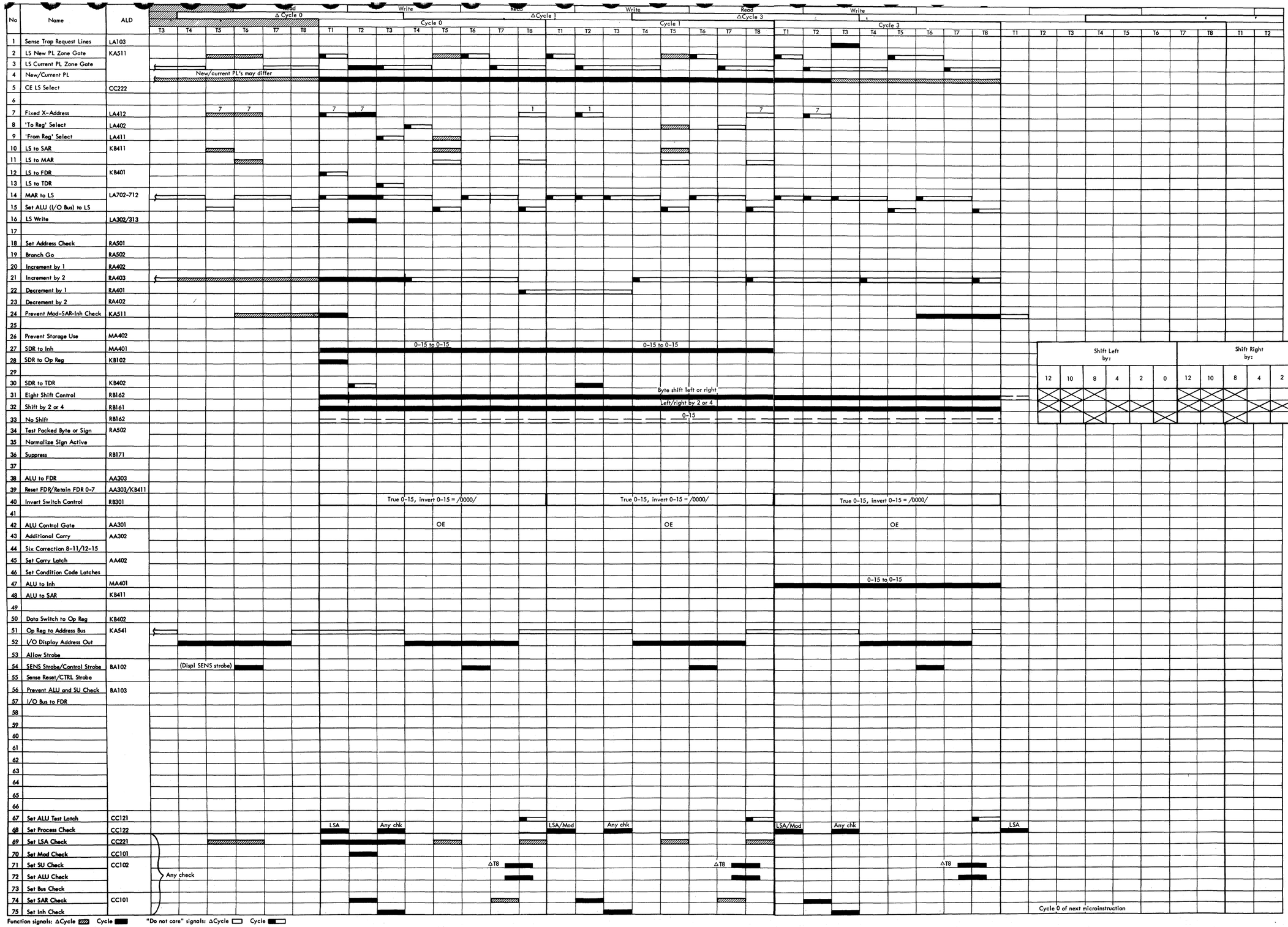


Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59		
60		
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	

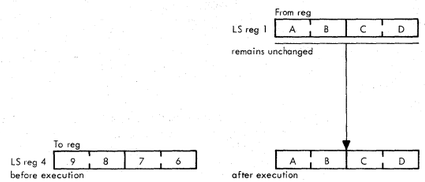


Shift Left by:						Shift Right by:					
12	10	8	4	2	0	12	10	8	4	2	0
X	X					X	X				
X	X	X				X	X	X			
X	X	X	X			X	X	X	X		
X	X	X	X	X		X	X	X	X	X	
X	X	X	X	X	X	X	X	X	X	X	X

Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▬

● Diagram 5-29. Shift Left/Right and Move (XX) (Part 2 of 2) (03734A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

The 'from reg' is moved into 'to reg'. The 'from reg' remains unchanged. Address check and the increment/decrement specification of operand addresses are ignored.



Microinstruction Layout

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Op Code						+ −	AC	To Reg				From Reg			
A			0	1				0				0			

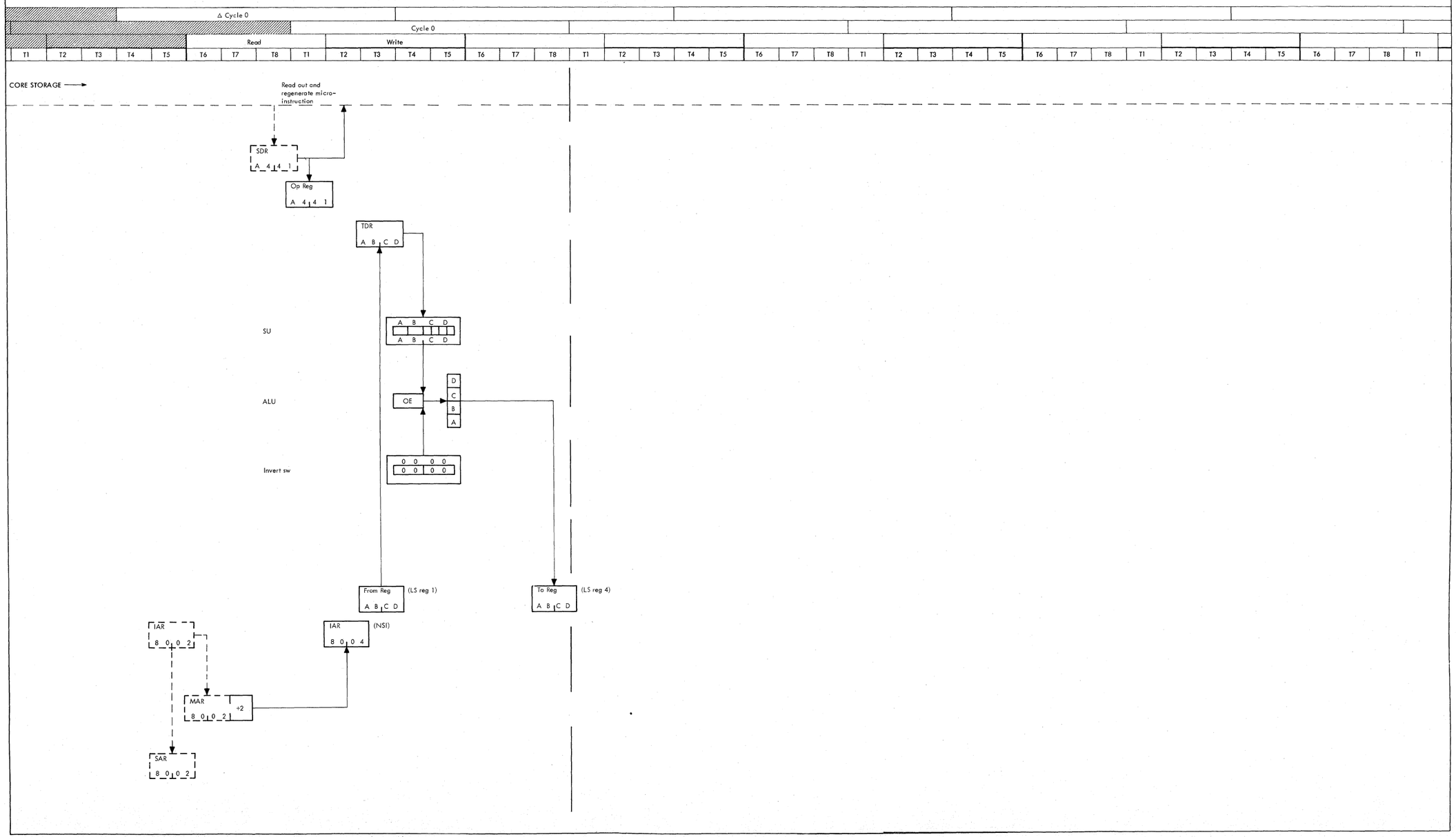
Ignored — + − — AC — To Reg — 0 — DD — From Reg — 0

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
A441	MVH	4,1	R4+= R1

Mnemonic
MVH
Format
FF
Type
DD

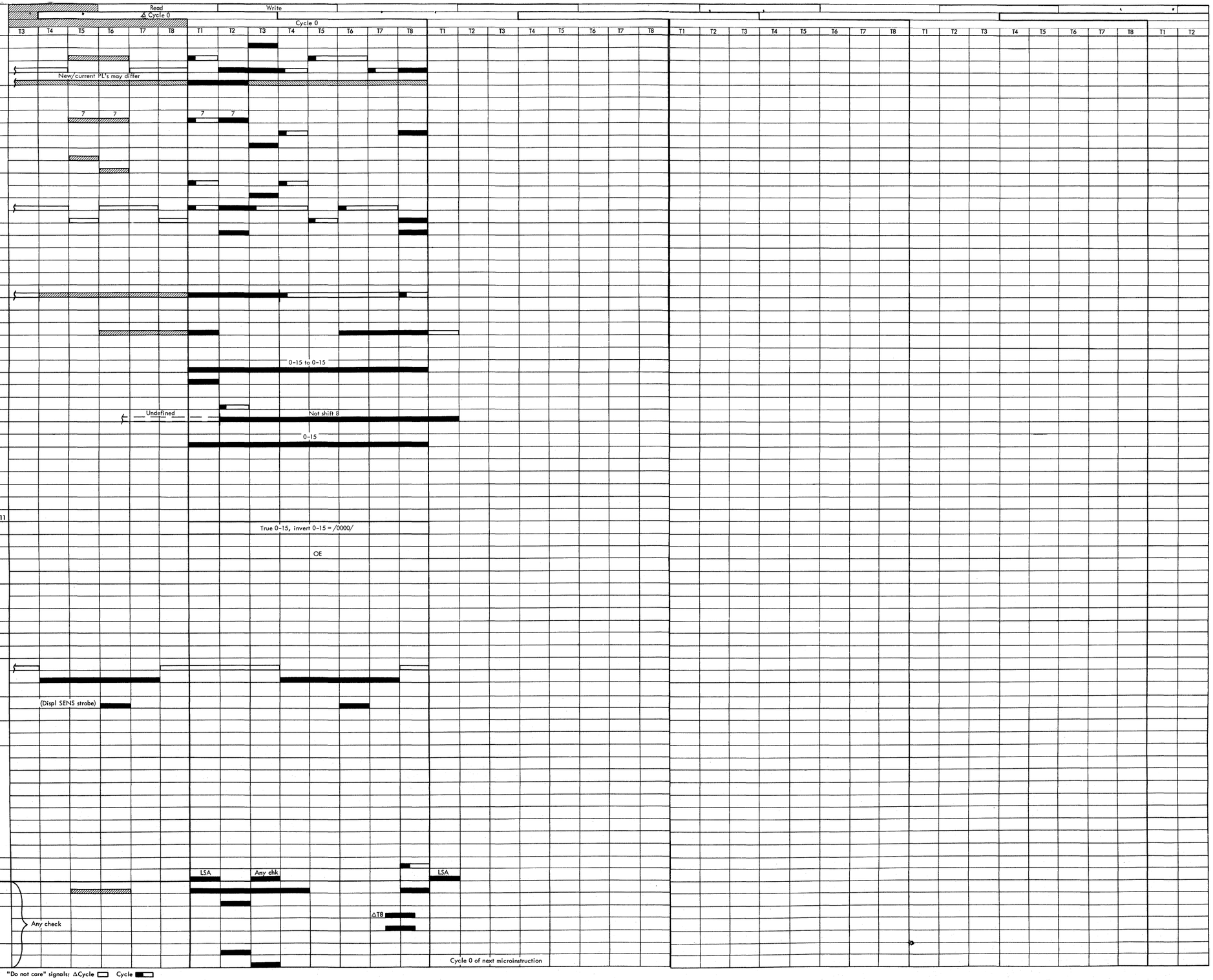
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
- Δ Cycle
- Cycle



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59		
60		
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	

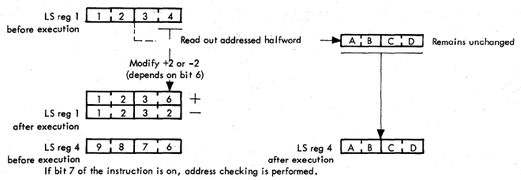


Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▭

Diagram 5-30. Move Halfword (DD) (Part 2 of 2) (03735A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

The halfword read out by the 'from reg' is moved into 'to reg'.

If the AC bit (instruction bit 7) is on, an address check occurs when the 'from reg' address is outside customer area or not on halfword boundary (not even). The 'from reg' address is incremented by 2 (instruction bit 6 on) or decremented by 2 (instruction bit 6 off).



Microinstruction Layout

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Op Code						±	AC	To Reg				From Reg			
A					0	1		0				1			

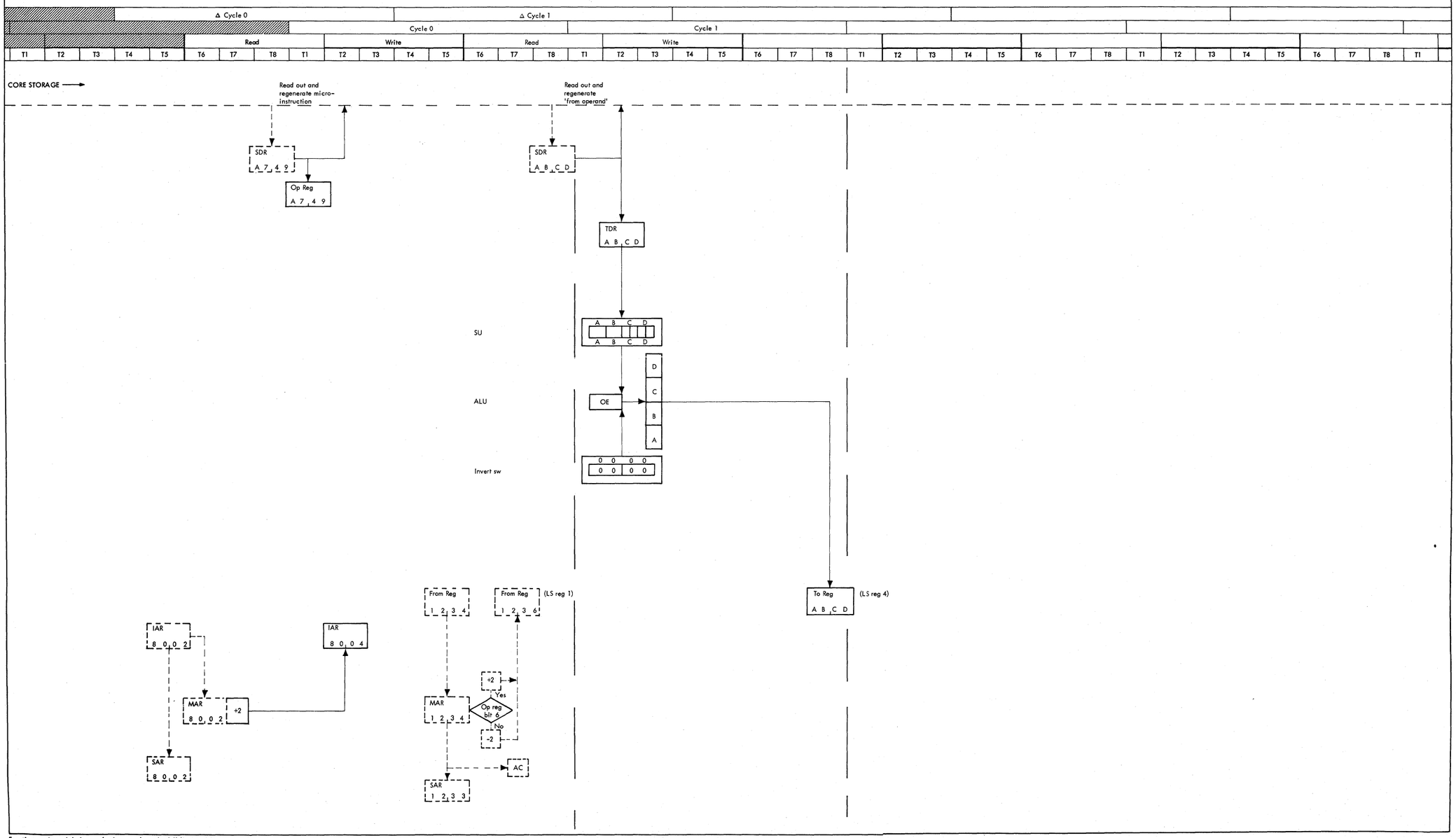
The 'from addr' is: incr by 2 if an decr by 2 if off

If on, the 'from addr' is checked that it is not outside customer area

DX

Mnemonic
MVH
Format
FF
Type
DX

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
A749	MVH	4,11,INC,AC	R4+= HW(R1,AC,+2)

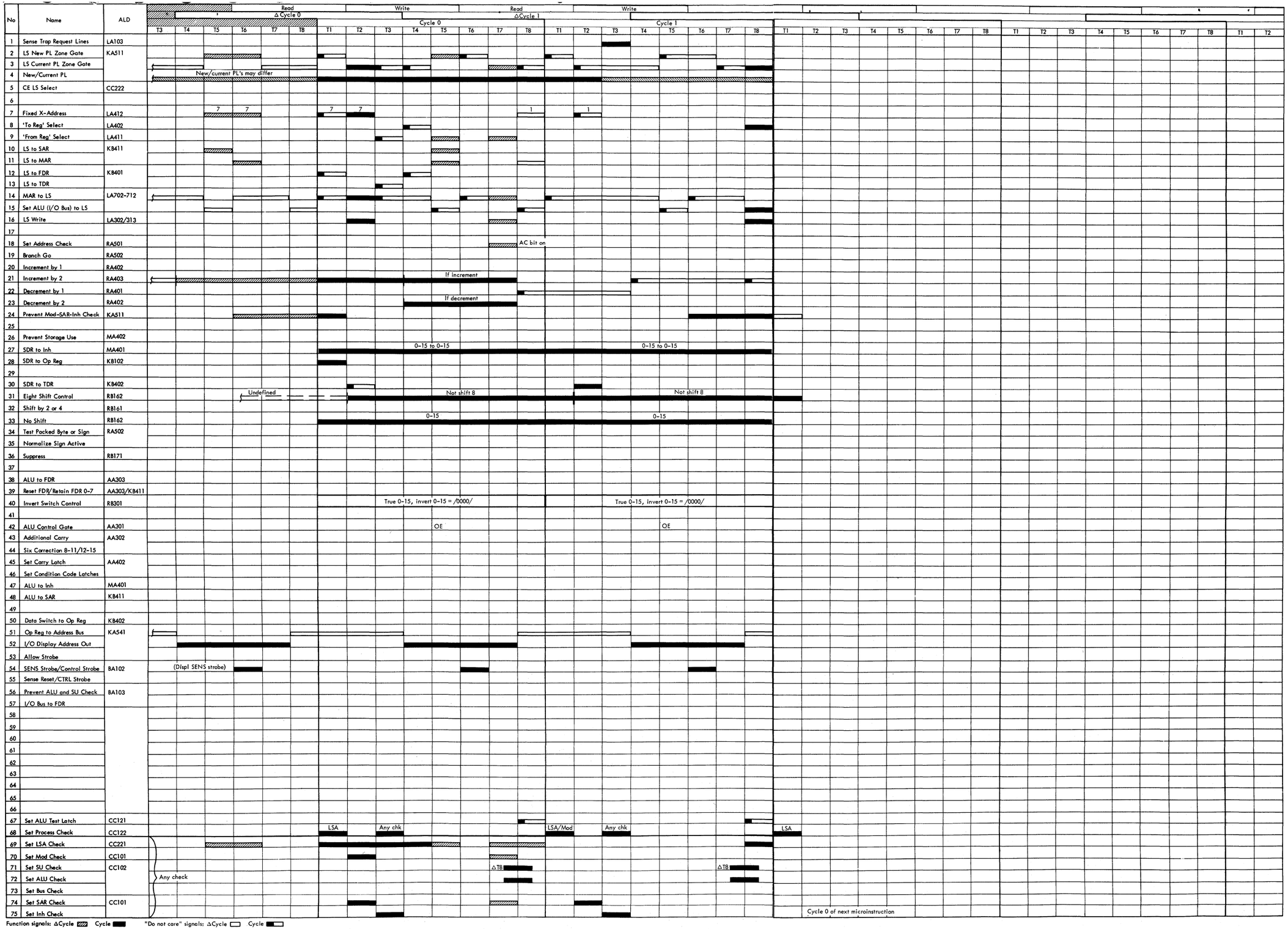


Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle

Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

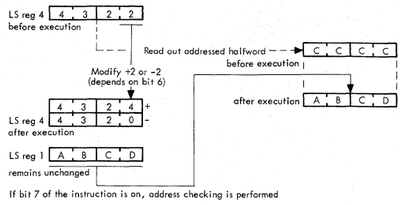
No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59		
60		
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▭

The 'from reg' is moved into the core storage halfword addressed by the 'to reg'. The 'from reg' remains unchanged. If the AC bit (instruction bit 7) is on, an address check occurs when the 'to reg' address is outside customer area or not on halfword boundary (not even).

The 'to reg' address is incremented by 2 (instruction bit 6 on) or decremented by 2 (instruction bit 6 off).



Microinstruction Layout

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Op Code						±	AC	To Reg				From Reg			
A				0	1			1				0			

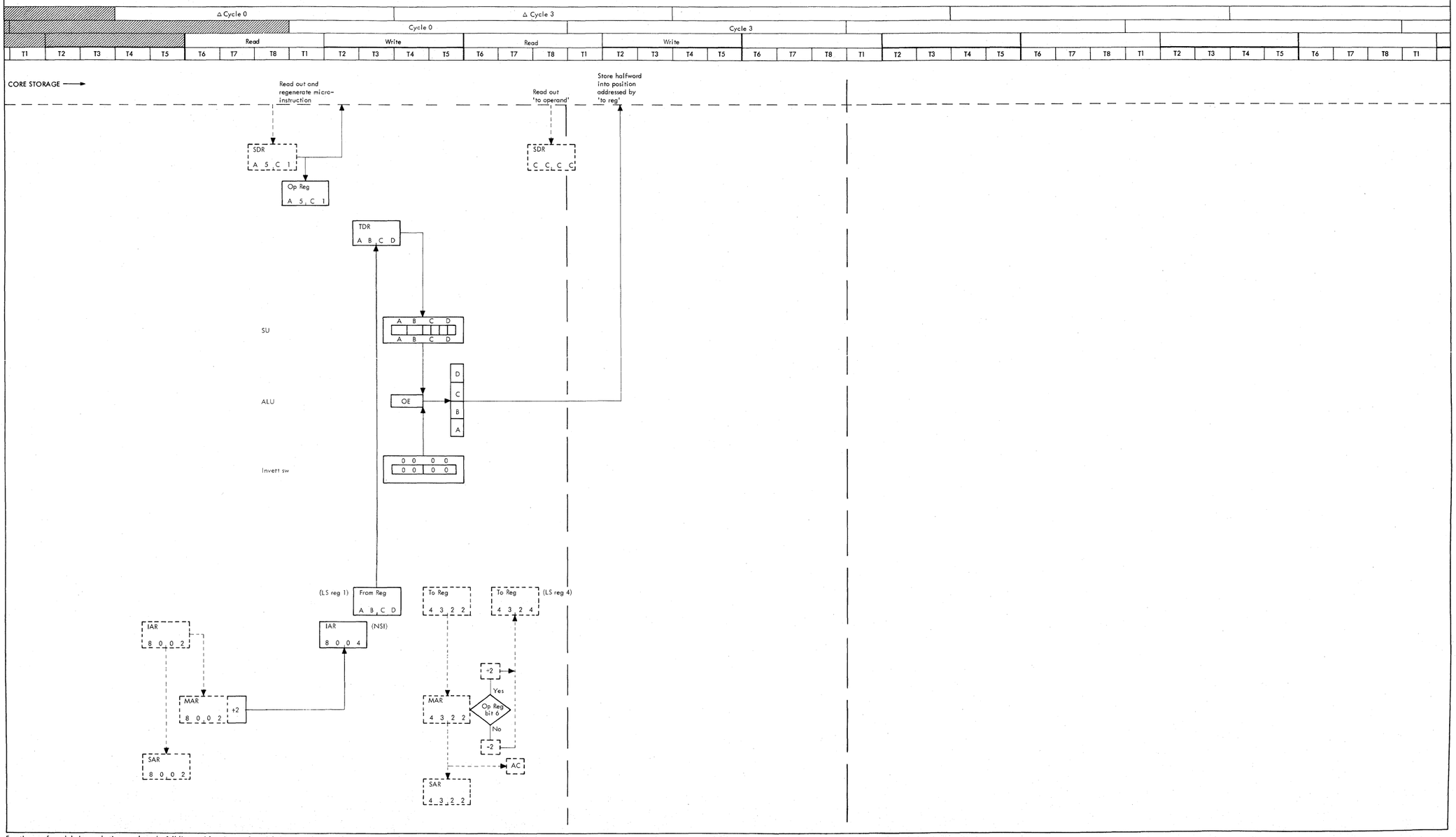
The 'to addr' is: incr by 2 if on, decr by 2 if off

If on the 'to addr' is checked that it is not outside customer area

XD

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
A5C1	MVH	4I,1,DEC,AC	HW(R4,AC,-2)+=R1

Mnemonic
MVH
Format
FF
Type
XD

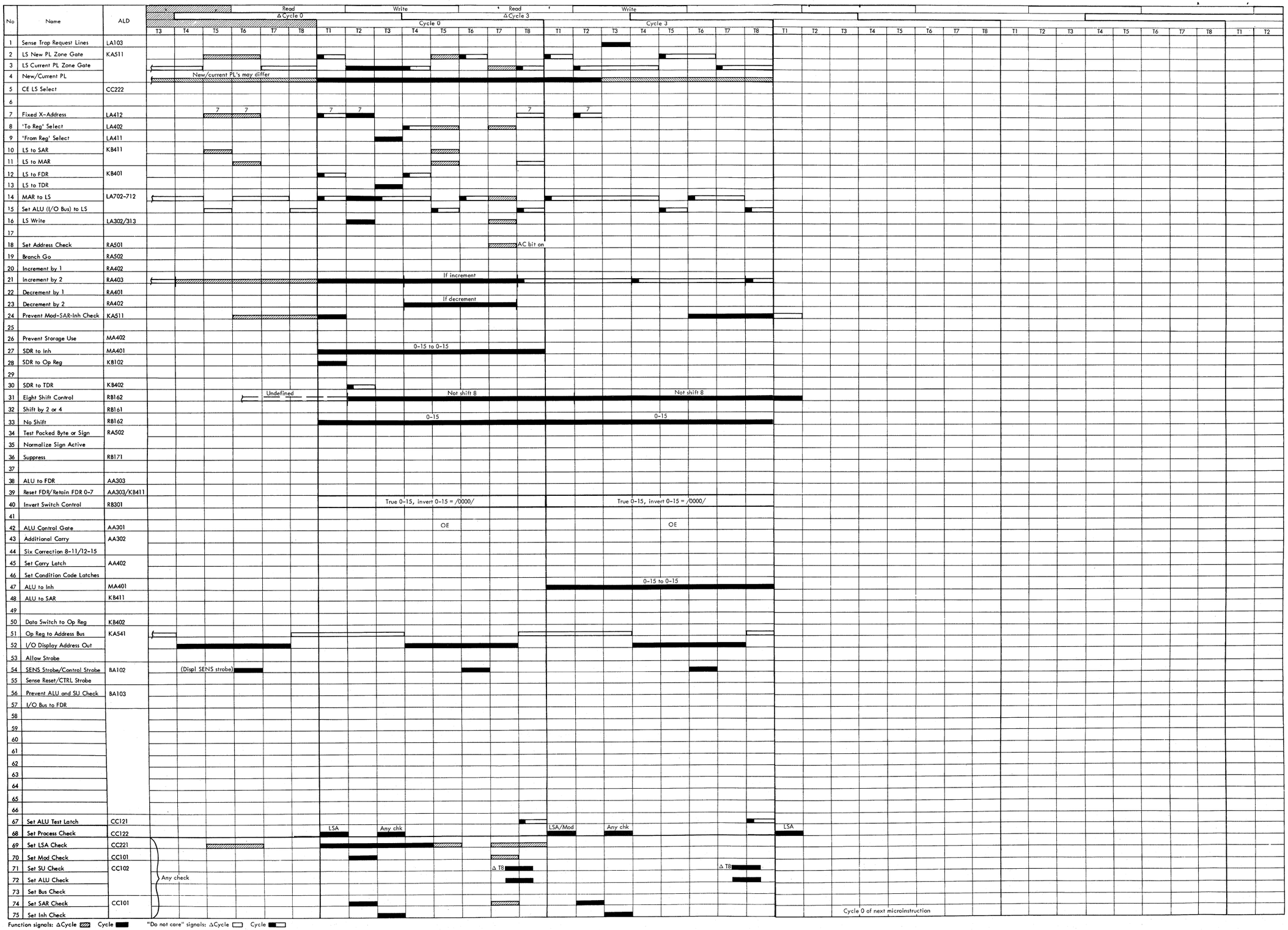


Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
Δ Cycle
Cycle

Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59		
60		
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	

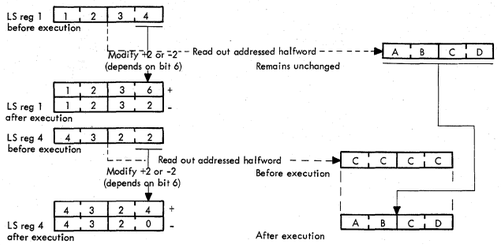


Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▬

The halfword addressed by the 'from reg' is moved into the halfword addressed by 'to reg' The 'from' halfword remains unchanged.

Both addresses are either incremented by 2 (instruction bit 6 on) or decremented by 2 (instruction bit 6 off). If the AC bit (instruction bit 7) is on, an address check occurs when the 'from reg' or 'to reg' address is outside customer area or not on halfword boundary.

The operation is performed in ALC mode when 'to reg' = 3 and 'from reg' = 5. LS register 1 contains the field length. The field length must reflect the number of bytes to be moved (always an even number) reduced by 2. For ALC, the operand addresses are updated according to instruction bit 6 (+2 or -2) every time a halfword is moved.



Microinstruction Layout

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Op Code						±	AC	To Reg				From Reg			
A				0	1			1				1			

The 'to' and 'from' addr's are: incr by 2 if on decr by 2 if off

If on, the 'to' and 'from' addr's are checked that they are not outside customer area.

XX

Mnemonic
MVH
Format
FF
Type
XX (ALC)

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
A5C9	MVH	4I,1I,DEC,AC	HW(R4,AC,-2)=HW(R1,AC,-2)
A7BD	MVH	3I,5I,INC, AC	HW(R3,AC,+2,UNTIL R1,LT,0)=HW(R5,AC,+2)

Repeat Δ Cycle 1 – Δ Cycle 3 — ALC end op — Yes → Δ Cycle 0 — No → Δ Cycle 3

Δ Cycle 0 | Δ Cycle 1 | Δ Cycle 3

Cycle 0 | Cycle 1 | Cycle 3

Read | Write | Read | Write | Read | Write

T1 T2 T3 T4 T5 T6 T7 T8 T1 T2 T3 T4 T5 T6 T7 T8 T1 T2 T3 T4 T5 T6 T7 T8 T1 T2 T3 T4 T5 T6 T7 T8 T1 T2 T3 T4 T5 T6 T7 T8 T1

CORE STORAGE →

Read out and regenerate micro-instruction

SDR A 5 C 9

Op Reg A 5 C 9

Read out and regenerate 'from operand'

SDR A B C D

TDR A B C D

Read out 'to operand'

SDR C C C C

Store halfword into position addressed by 'to reg'

SU

A B C D
A B C D

ALU

D C B A

OE

Invert sw

0 0 0 0
0 0 0 0

IAR 8 0 0 2

MAR 8 0 0 2 +2

ALC — No → IAR 8 0 0 4 (NSI); Yes → No action

SAR 8 0 0 2

(LS reg 1) From Reg 1 2 3 4

From Reg 1 2 3 2

MAR 1 2 3 4

Op reg bit 6 — Yes → +2 → MAR; No → -2 → MAR

AC

SAR 1 2 3 4

LS Reg 1 0 0 0 8

MAR 0 0 0 8 -2

ALC — Yes → LS Reg 1 0 0 0 6; No → No action

Decrement Carry 0 forces ALC end op

(LS reg 4) To Reg 4 3 2 2

To Reg 4 3 2 0

MAR 4 3 2 2

Op reg bit 6 — Yes → +2 → MAR; No → -2 → MAR

AC

SAR 4 3 2 2

IAR 8 0 0 2

MAR 8 0 0 2 +2

ALC end op — Yes → IAR 8 0 0 4 (NSI); No → No action

Note: For "Do not care" functions refer to timing chart below.

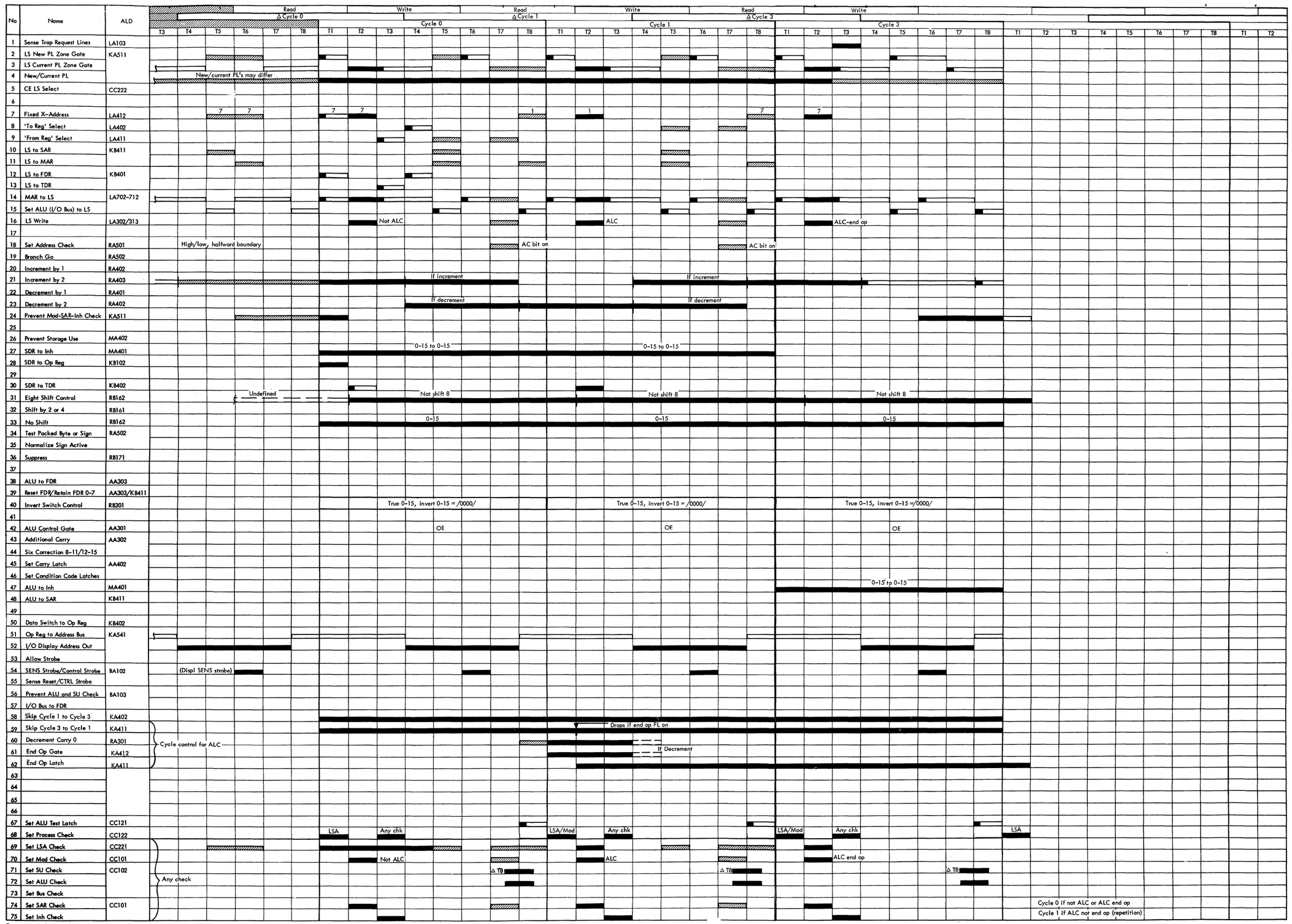
"Do not care" signals:
ΔCycle
Cycle

Functions performed during cycle time are shown by full lines and functions performed durina Δ cycle time are shown by dotted lines.

03738 A

Diagram 5-33. Move Halfword (XX, ALC) (Part 1 of 2) (03738A)

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58	Skip Cycle 1 to Cycle 3	KA402
59	Skip Cycle 3 to Cycle 1	KA411
60	Decrement Carry 0	RA301
61	End Op Gate	KA412
62	End Op Latch	KA411
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	

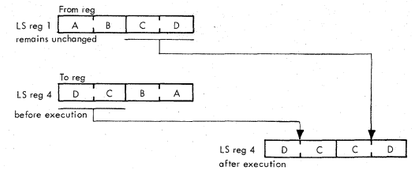


Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ■

● Diagram 5-33. Move Halfword (XX, ALC) (Part 2 of 2) (03738A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

The low-order byte of the 'from reg' is moved into the low-order byte of the 'to reg'.

'From reg' and high-order byte of 'to reg' remain unchanged. Address check and increment/ decrement specification of operand addresses are ignored.



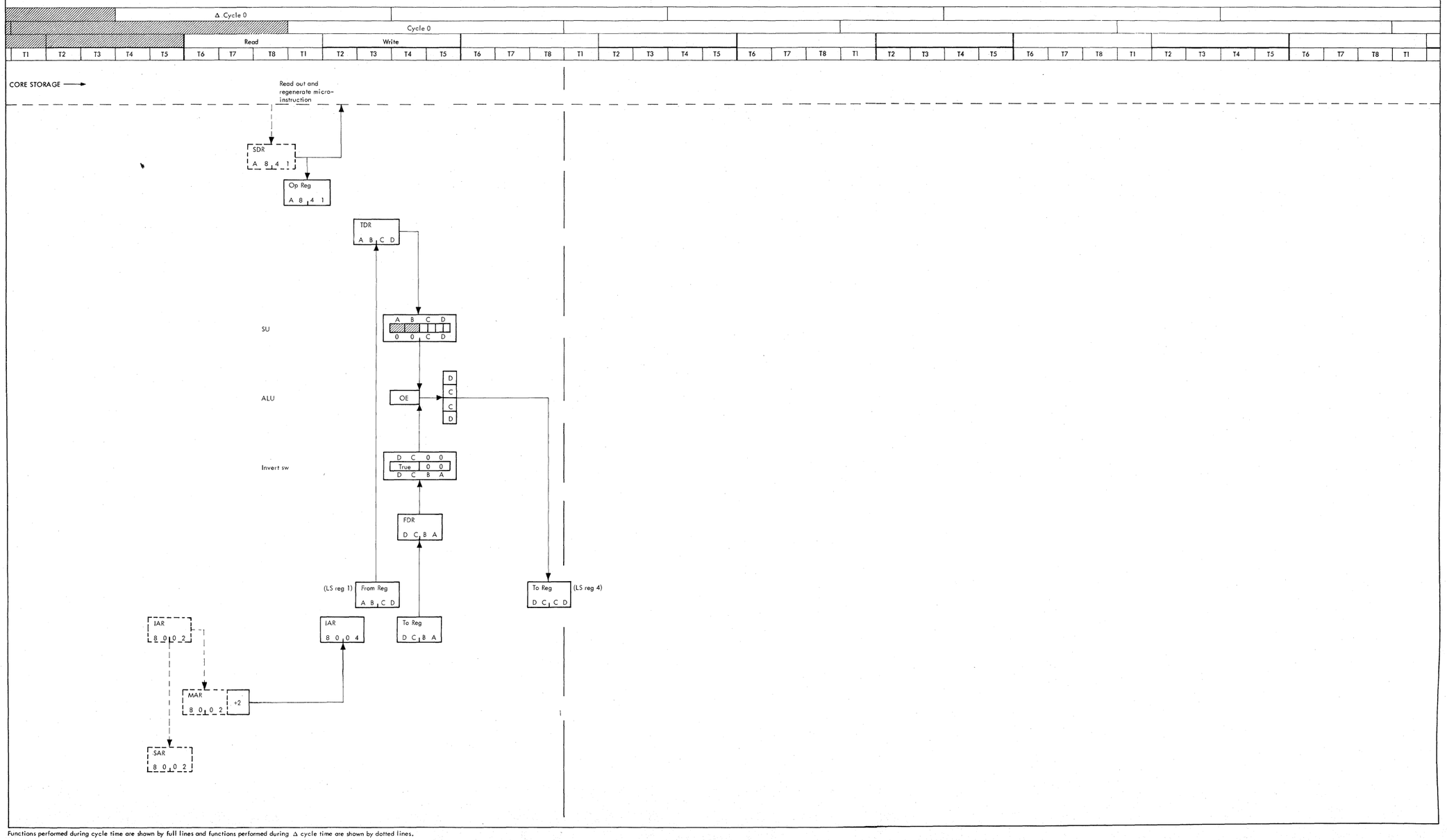
Microinstruction Layout

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Op Code						±	AC	To Reg				From Reg			
A					1	0			0			0			

Ignored — DD

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
A841	MVB	4,1	R4+=R4.0-7/R1.8-15

Mnemonic
MVB
Format
FF
Type
DD

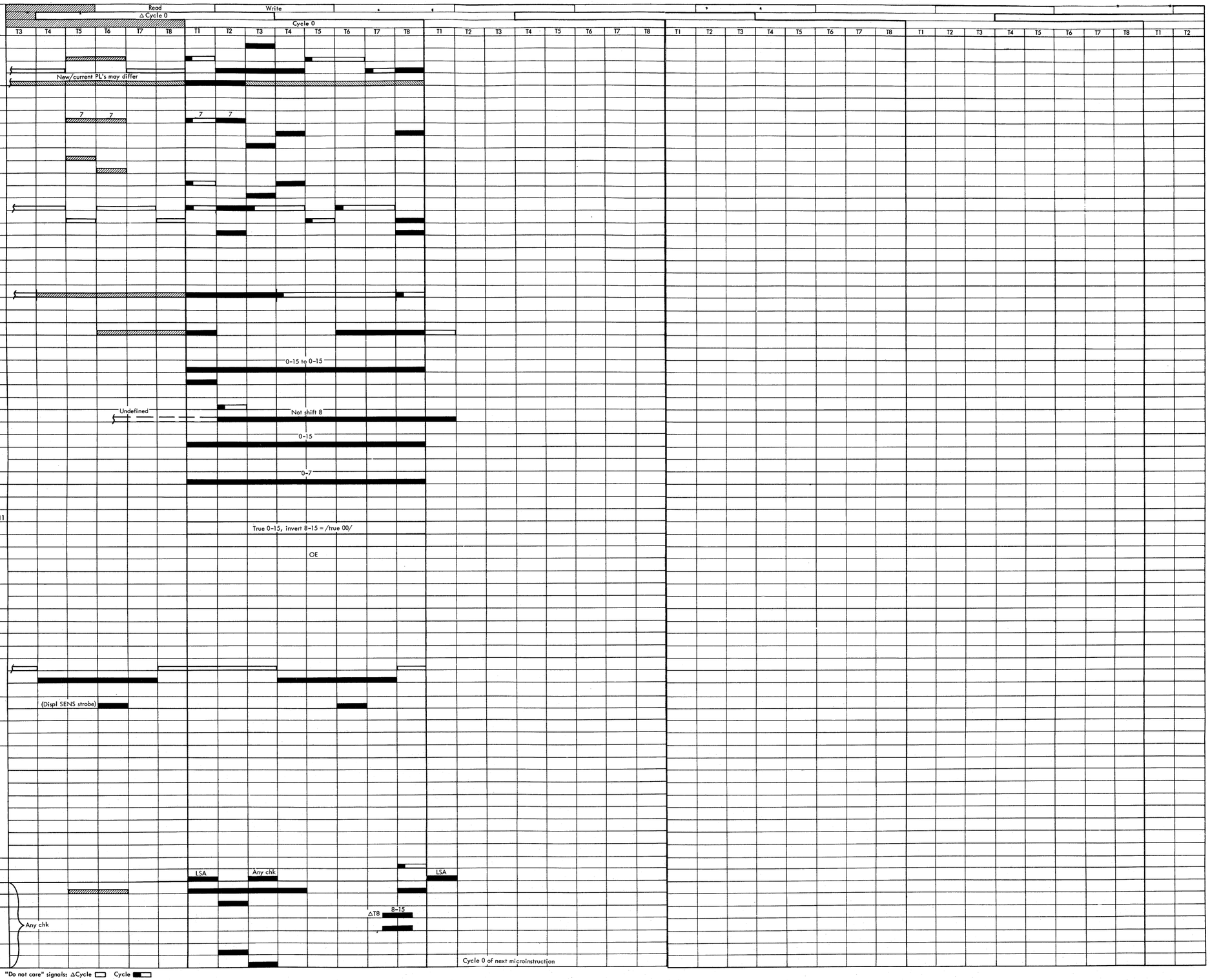


Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle

Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59		
60		
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	

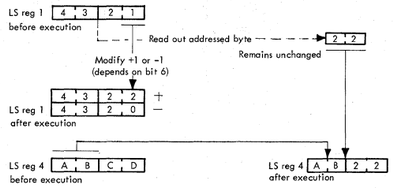


Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▭

● Diagram 5-34. Move Byte (DD) (Part 2 of 2) (03739A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

The byte addressed by the 'from reg' is moved into the low-order byte of the 'to reg'. The 'from' byte and the high-order byte of 'to reg' remain unchanged. If the AC bit (instruction bit 7) is on, an address check occurs when the 'from reg' address is outside customer area.

The 'from reg' address is incremented by 1 (instruction bit 6 on) or decremented by 1 (instruction bit 6 off)



Microinstruction Layout

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Op Code						±	AC	To Reg				From Reg			
A					1	0		0				1			

The 'from addr' is: incr by 1 if on, decr by 1 if off

If on, the 'from'addr is checked that it is not outside customer area

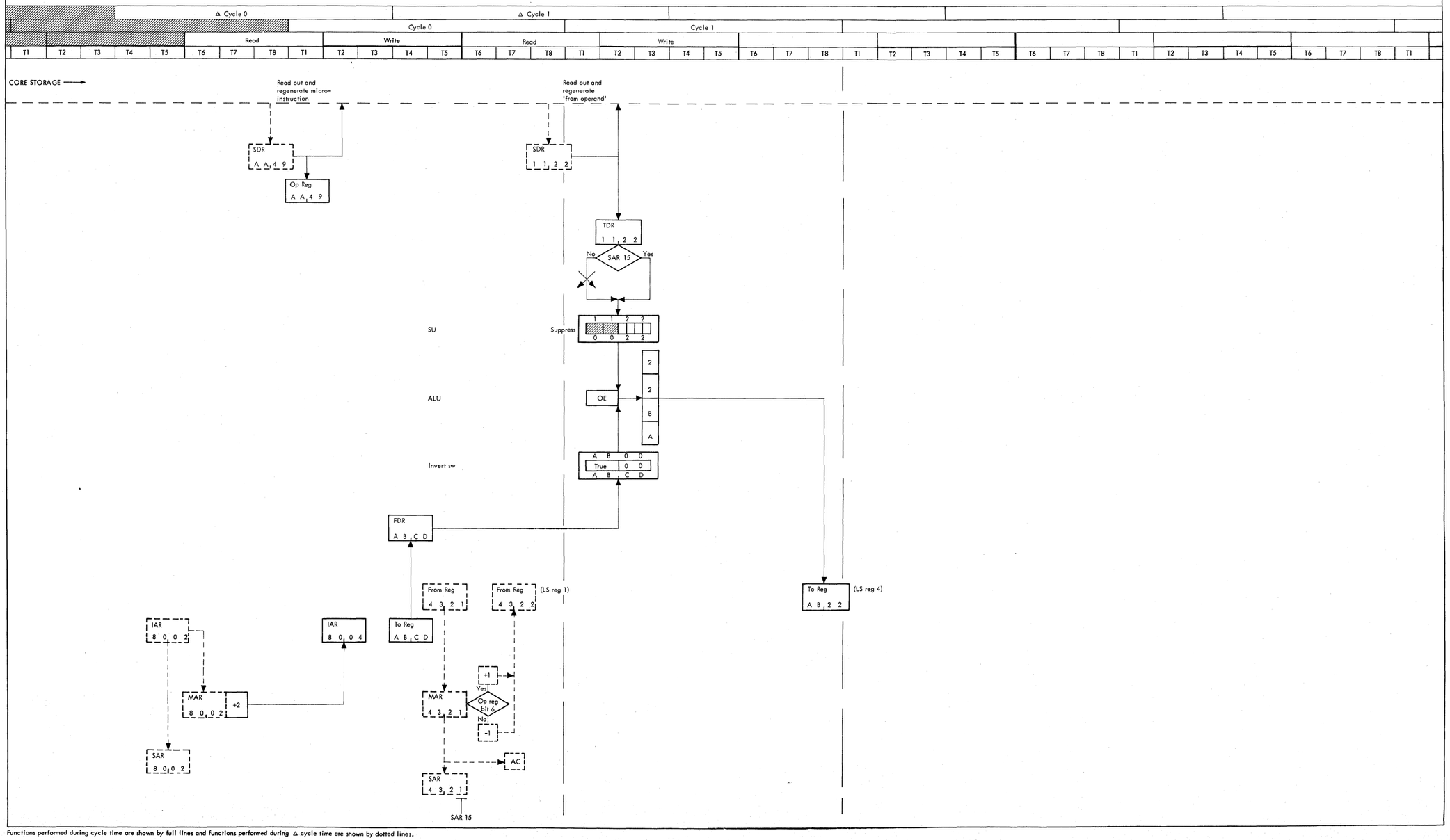
DX

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
AA49	MVB	4,11,INC	R4+=R4.0-7/BY(R1,+1)

Mnemonic
MVB
Format
FF
Type
DX

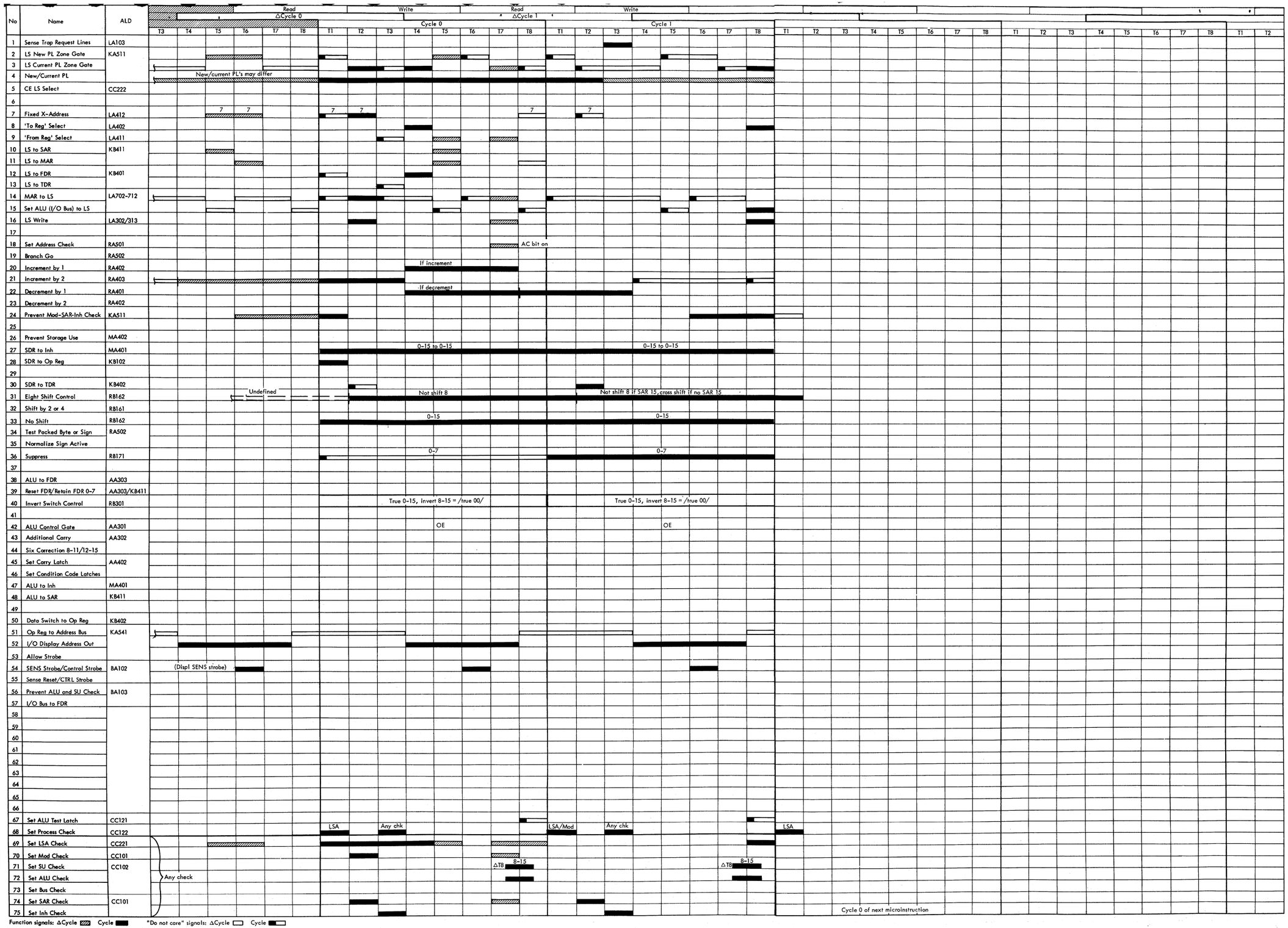
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

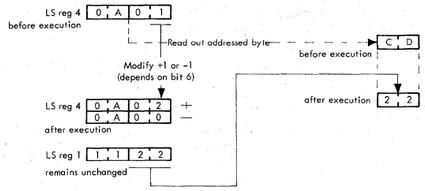
No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59		
60		
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	

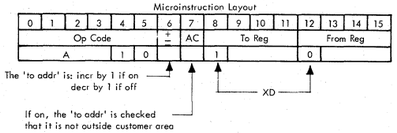


Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▭

The low-order byte of the 'from reg' is moved into the byte addressed by the 'to reg'. The 'from reg' remains unchanged. If the AC bit (instruction bit 7) is on, an address check occurs when the 'to reg' address is outside customer area.

The 'to reg' address is incremented by 1 (instruction bit 6 on) or decremented by 1 (instruction bit 6 off).



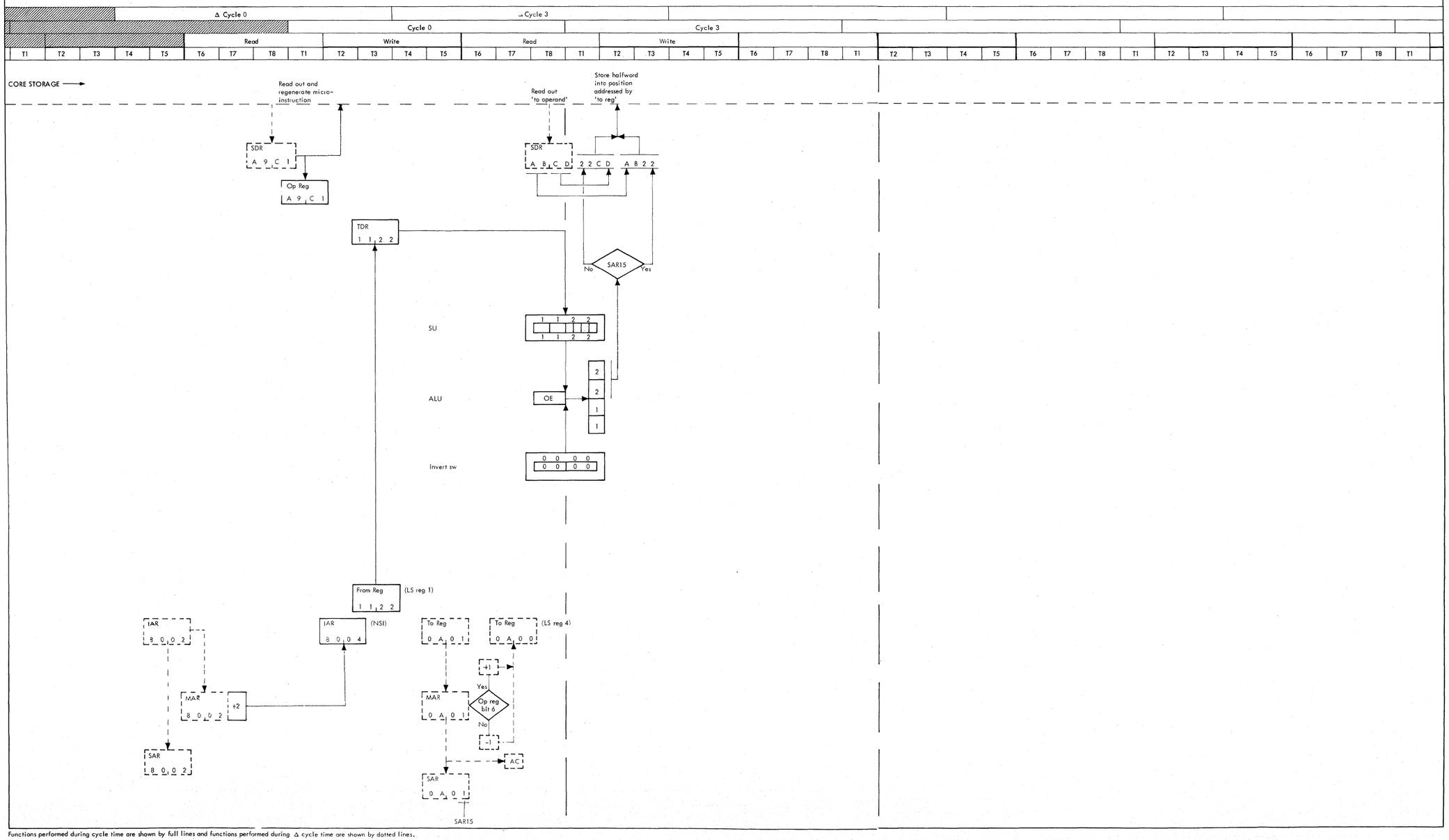


INST	NAME	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
A9C1	MVB	4I,1,D-S,AC	BY(R4,AC,-1)+=R1.8-15

Mnemonic
MVB
Format
FF
Type
XD

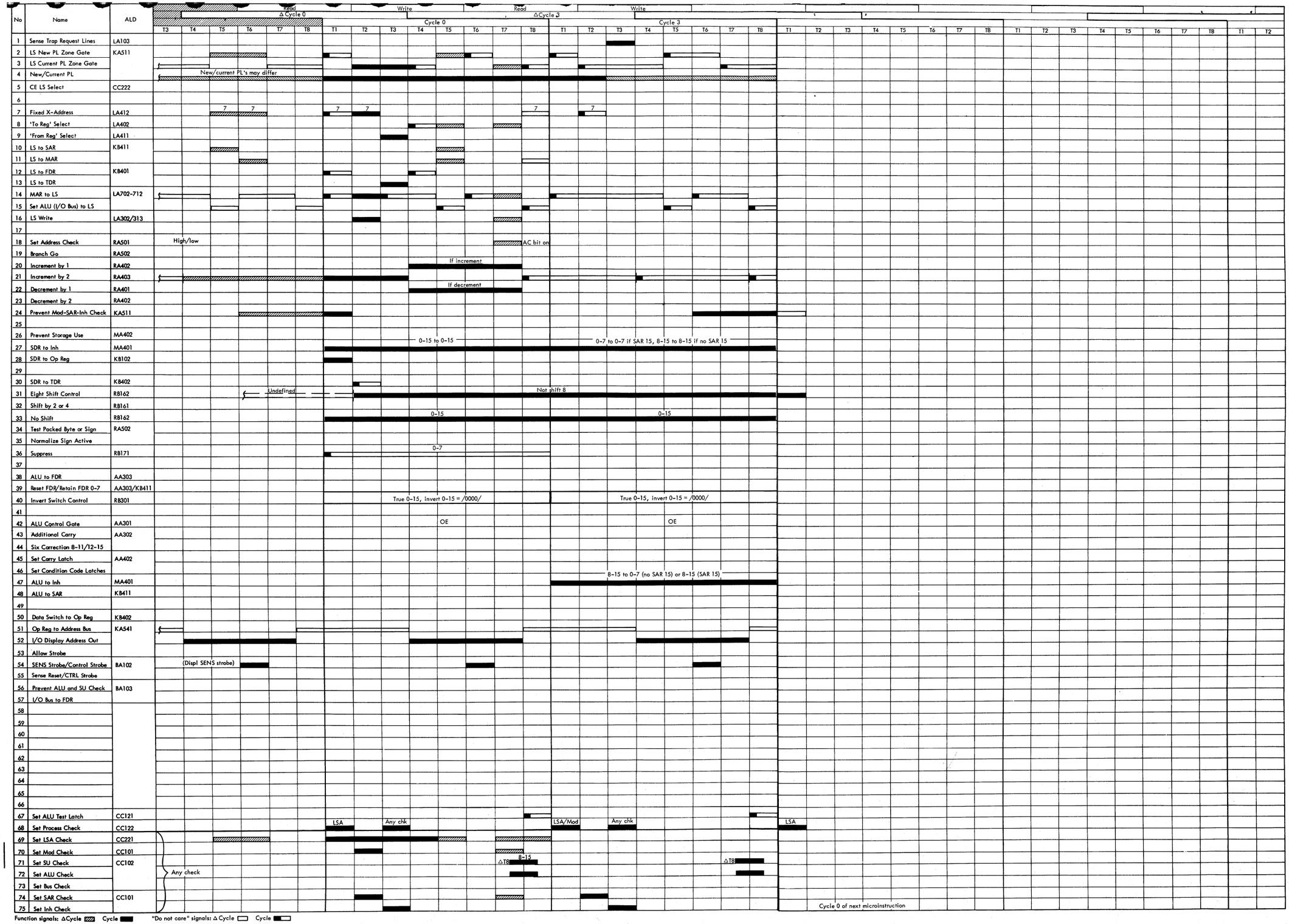
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59		
60		
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	

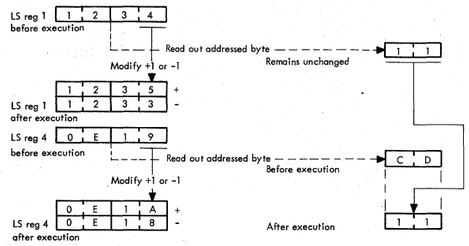


● **Diagram 5-36. Move Byte (XD) (Part 2 of 2)** (03741A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

The byte addressed by the 'from reg' is moved into the byte addressed by the 'to reg'.

The 'from' byte remains unchanged. Both addresses are either incremented by 1 (instruction bit 6 on) or decremented by 1 (instruction bit 6 off). If the AC bit (instruction bit 7) is on, an address check occurs when the 'from reg' or 'to reg' address is outside customer area.

The operation is performed in ALC mode when 'to reg' = 3 and 'from reg' = 5. LS register 1 contains the field length. The field length is the real number of bytes to be moved, reduced by 1. For ALC, the operand addresses are updated according to instruction bit 6 (+1 or -1) every time a byte is moved.



Microinstruction Layout

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Op Code						±	AC	To Reg				From Reg			
A				1	0			1				1			

The 'to' and 'from' addr's are: incr by 1 if on, decr by 1 if off.
If on, the 'from' and 'to' addr's are checked that they are not outside customer area

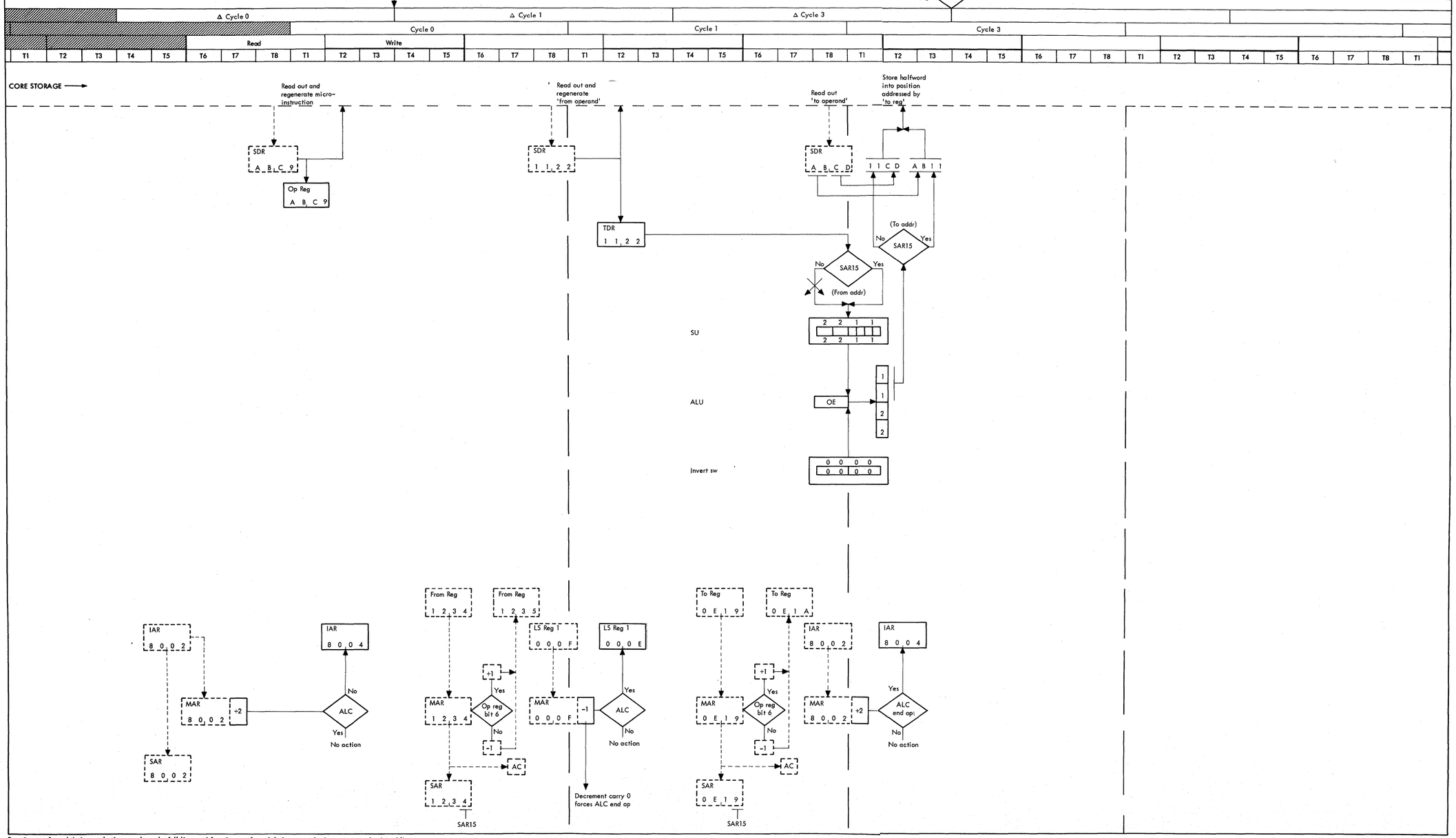
XX

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD GEB 0-1046-XXX
ABC9	MVB	4I,1I,INC,AC	BY(R4,AC,+1)=BY(R1,AC,+1)
ABBD	MVB	3I,5I,INC,AC	BY(R3,AC,+1,UNTIL R1,LT,0)=BY(R5,AC,+1)

Mnemonic
MVB
Format
FF
Type
XX (ALC)

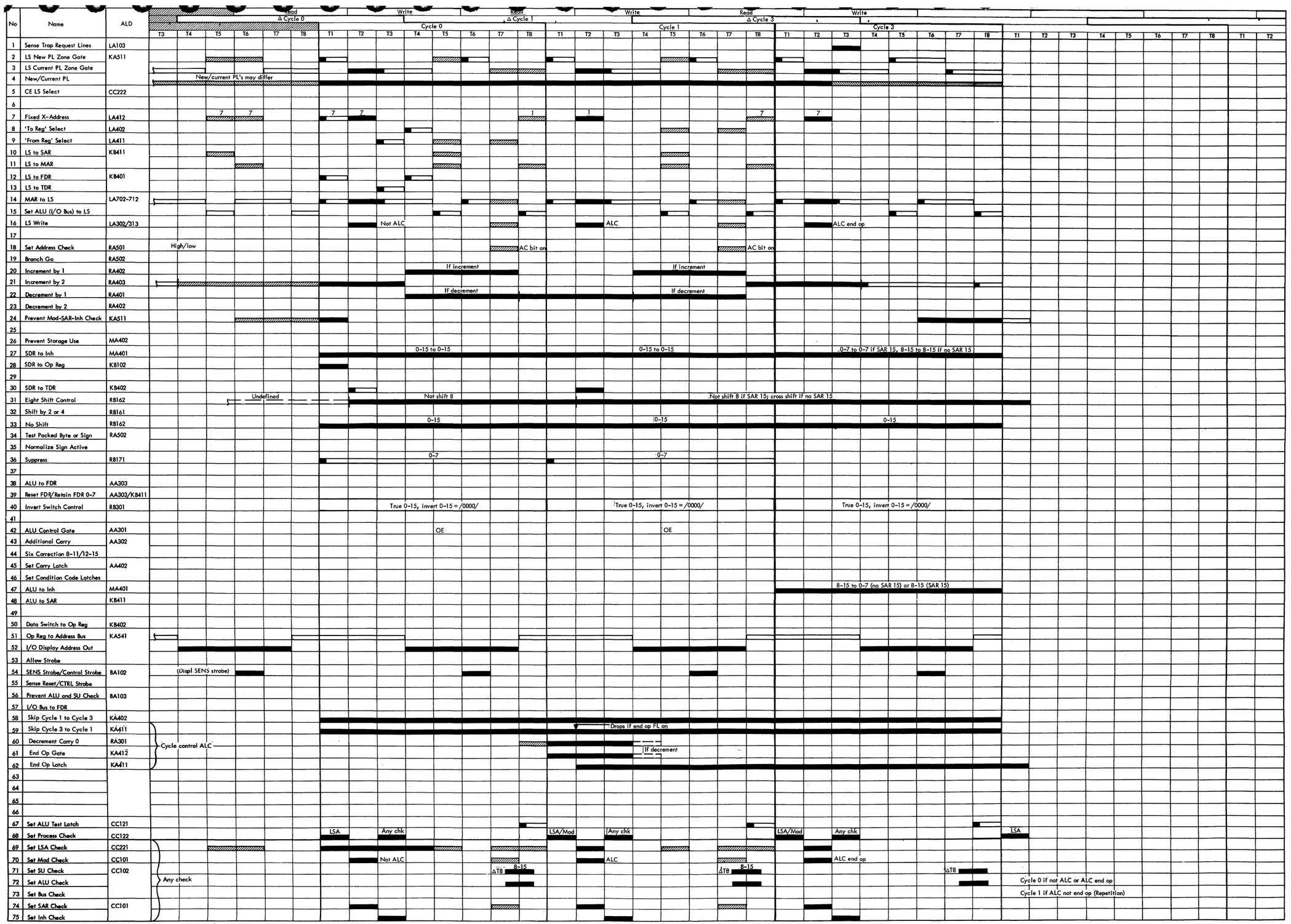
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58	Skip Cycle 1 to Cycle 3	KA402
59	Skip Cycle 3 to Cycle 1	KA411
60	Decrement Carry 0	RA301
61	End Op Gate	KA412
62	End Op Latch	KA411
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	

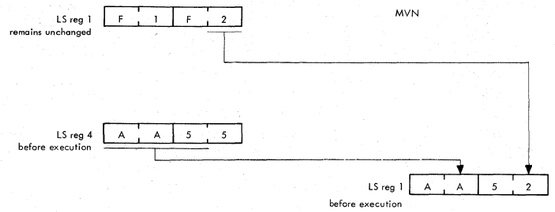


Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▭

● Diagram 5-37. Move Byte (XX, ALC) (Part 2 of 2) (03742A)

The numeric (zone) of the low-order byte of the 'from reg' is moved into the numeric (zone) of the low-order byte of the 'to reg'.

The 'from reg', the highorder byte of the 'to reg', and the zone (numeric) of low-order byte of the 'to reg' remain unchanged. Address check is ignored.



Microinstruction Layout

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
Op Code							AC	To Reg				From Reg				
A		1	1	0			0					0				MVN
A		1	1	1			0					0				MVZ

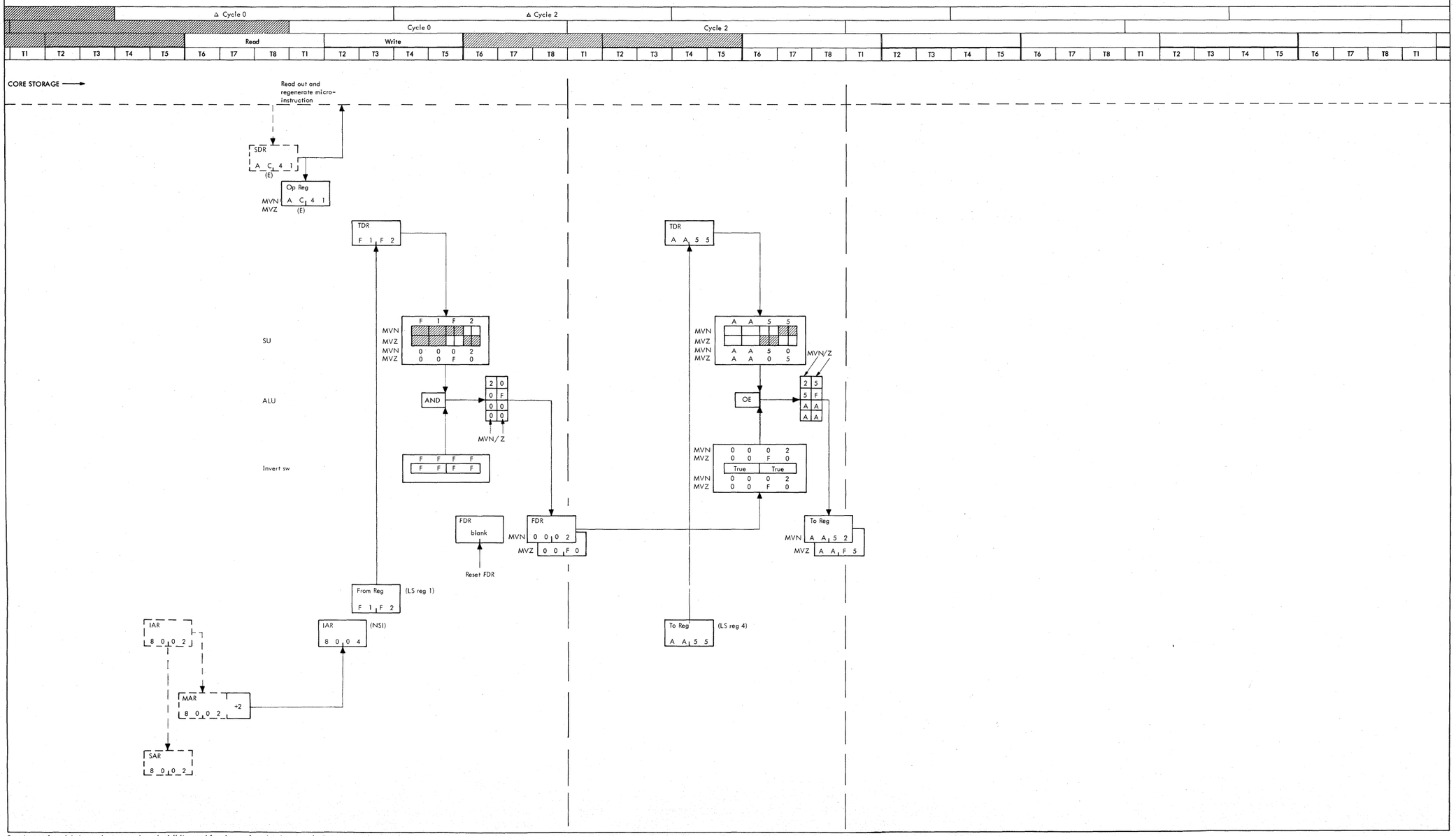
Ignored — DD

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
AC41	MVN	4,1	R4+=R4.0-11/R1.12-15
AE41	MVZ	4,1	R4+=R4.0-7/R1.8-11/R4.12-15

Mnemonic
MVN
MVZ
Format
FF
Type
DD

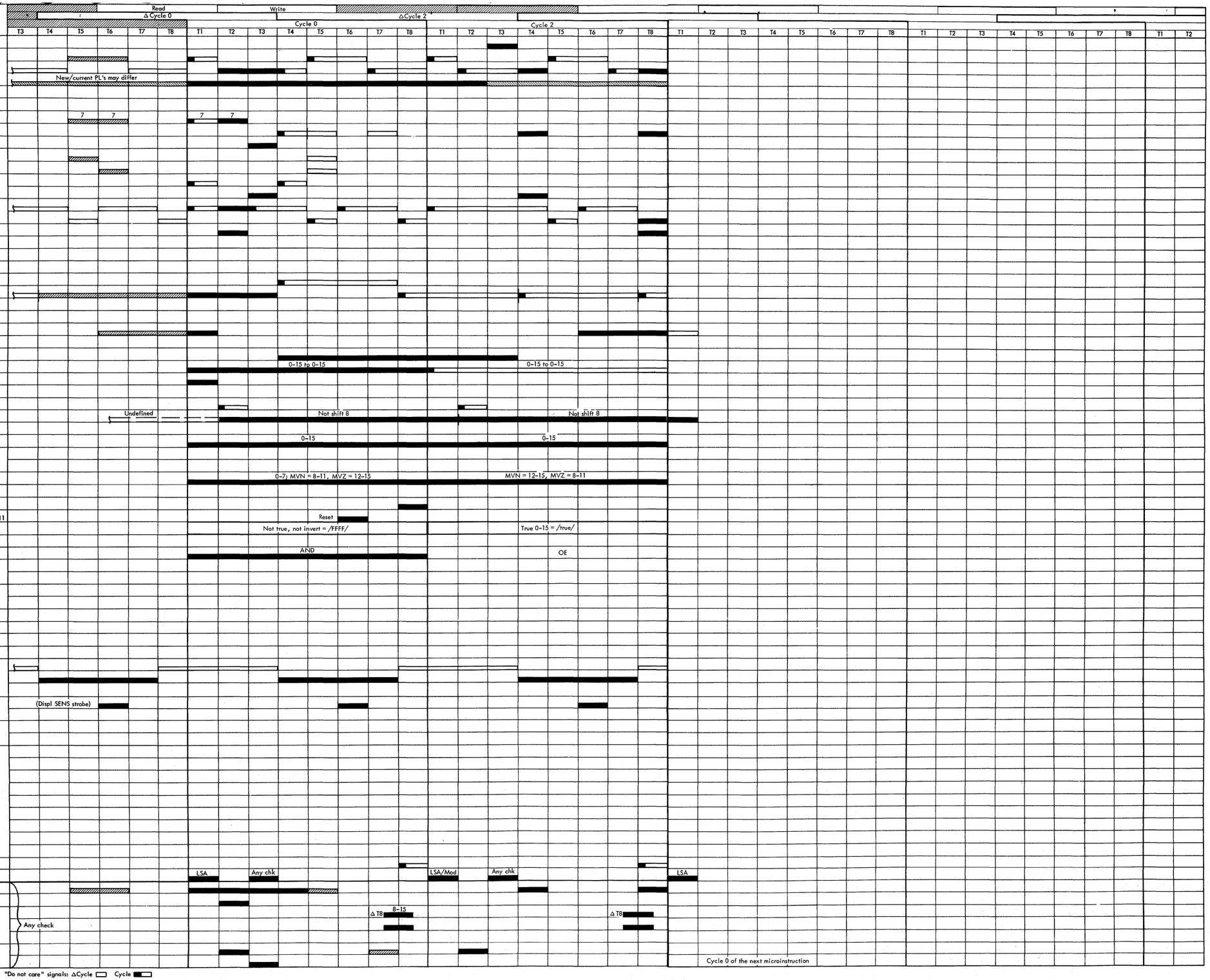
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
14	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59		
60		
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



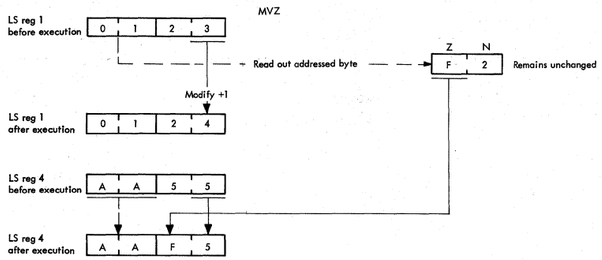
Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▬

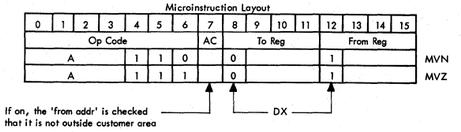
The numeric (zone) of the byte addressed by the 'from reg' is moved into the numeric (zone) of the low-order byte of the 'to reg'.

The 'from' byte, high-order byte of the 'to reg', and the zone (numeric) of the low-order byte of the 'to reg' remain unchanged.

The 'from reg' address is incremented by 1.

If the AC bit (instruction bit 7) is on, an address check occurs when the 'from reg' address is outside customer area.



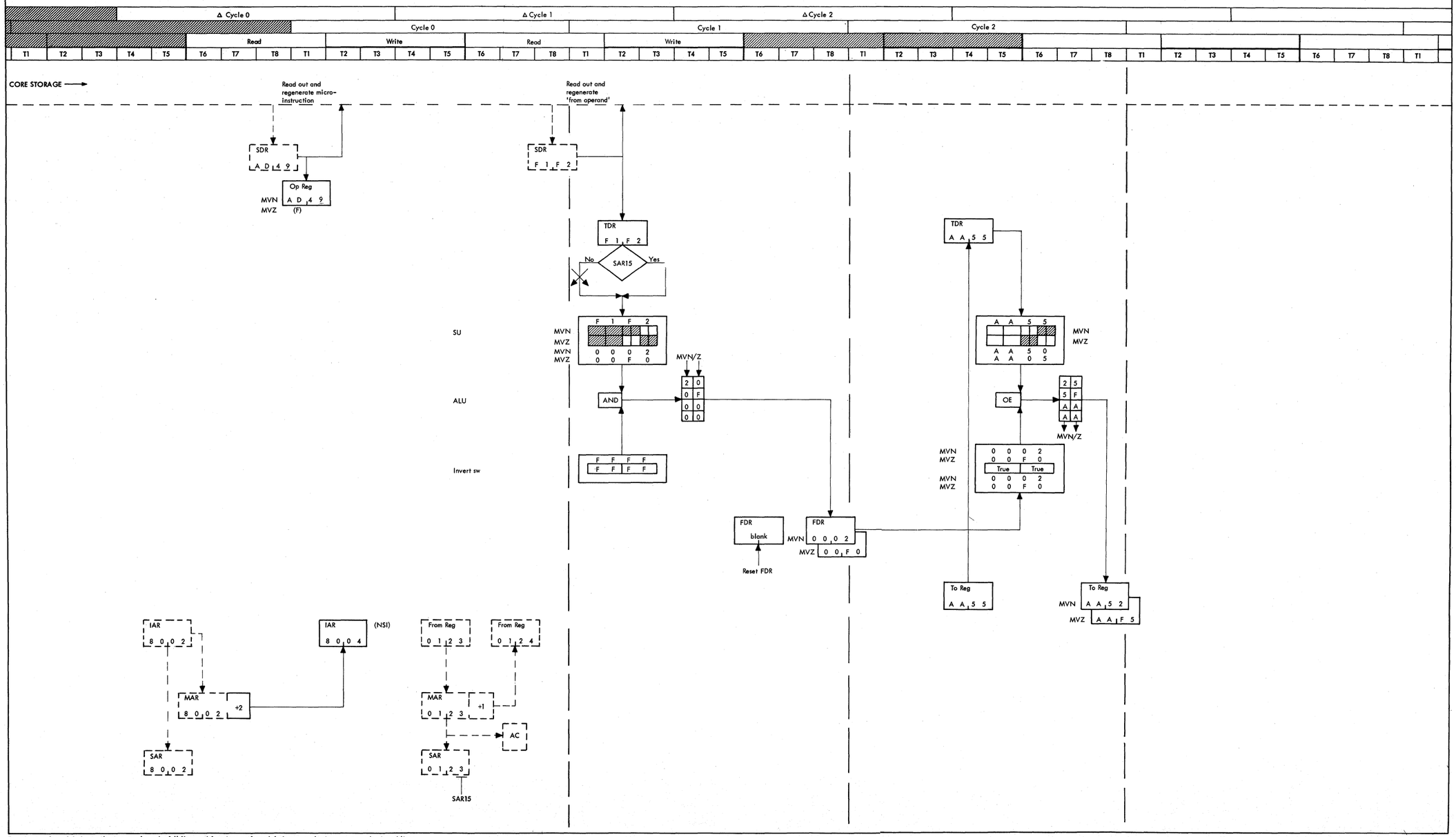


INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
AD49	MVN	4,11,AC	R4+=R4.0-11/BY(R1,AC,+1).4-7
AF49	MVZ	4,11,AC	R4+=R4.0-7/BY(R1,AC,+1).0-3/R4.12-15

Mnemonic
MVN
MVZ
Format
FF
Type
DX

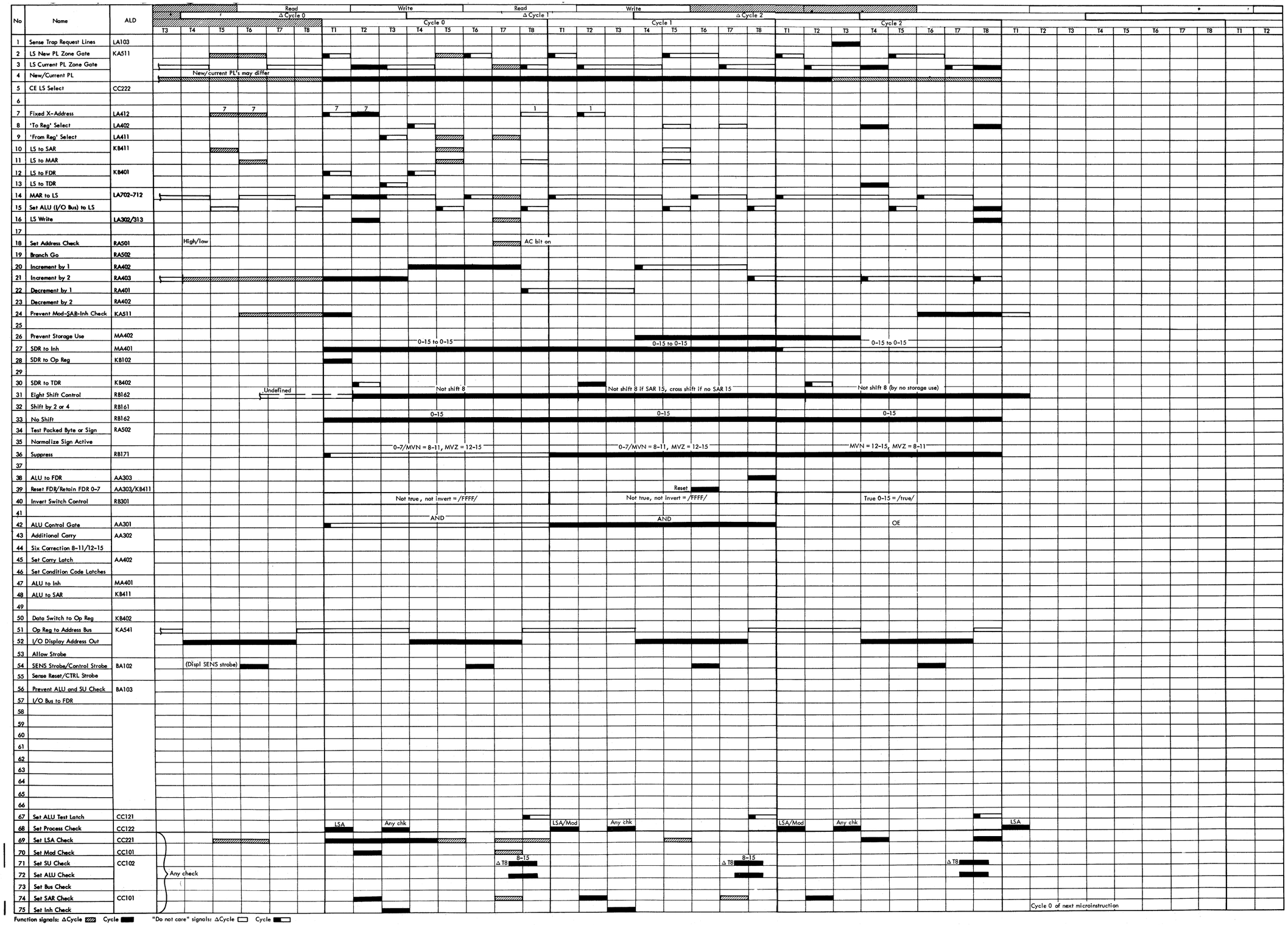
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
- Δ Cycle
- Cycle



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59		
60		
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	

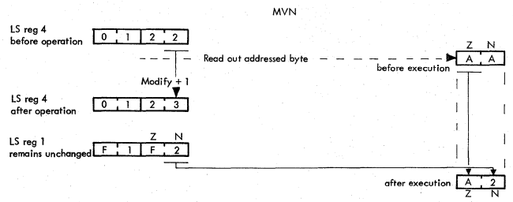


Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▭

The numeric (zone) of the low-order byte of the 'from reg' is moved into the numeric (zone) of the byte addressed by the 'to reg'.

The 'from reg' and the zone (numeric) of the 'to' byte remain unchanged.

The 'to reg' address is incremented by 1. If the AC bit (instruction bit 7) is on, an address check occurs when the 'to reg' address is outside customer area.



Microinstruction Layout

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
Op Code							AC	To Reg				From Reg				
A			1	1	0		1					0				MVN
A			1	1	1		1					0				MVZ

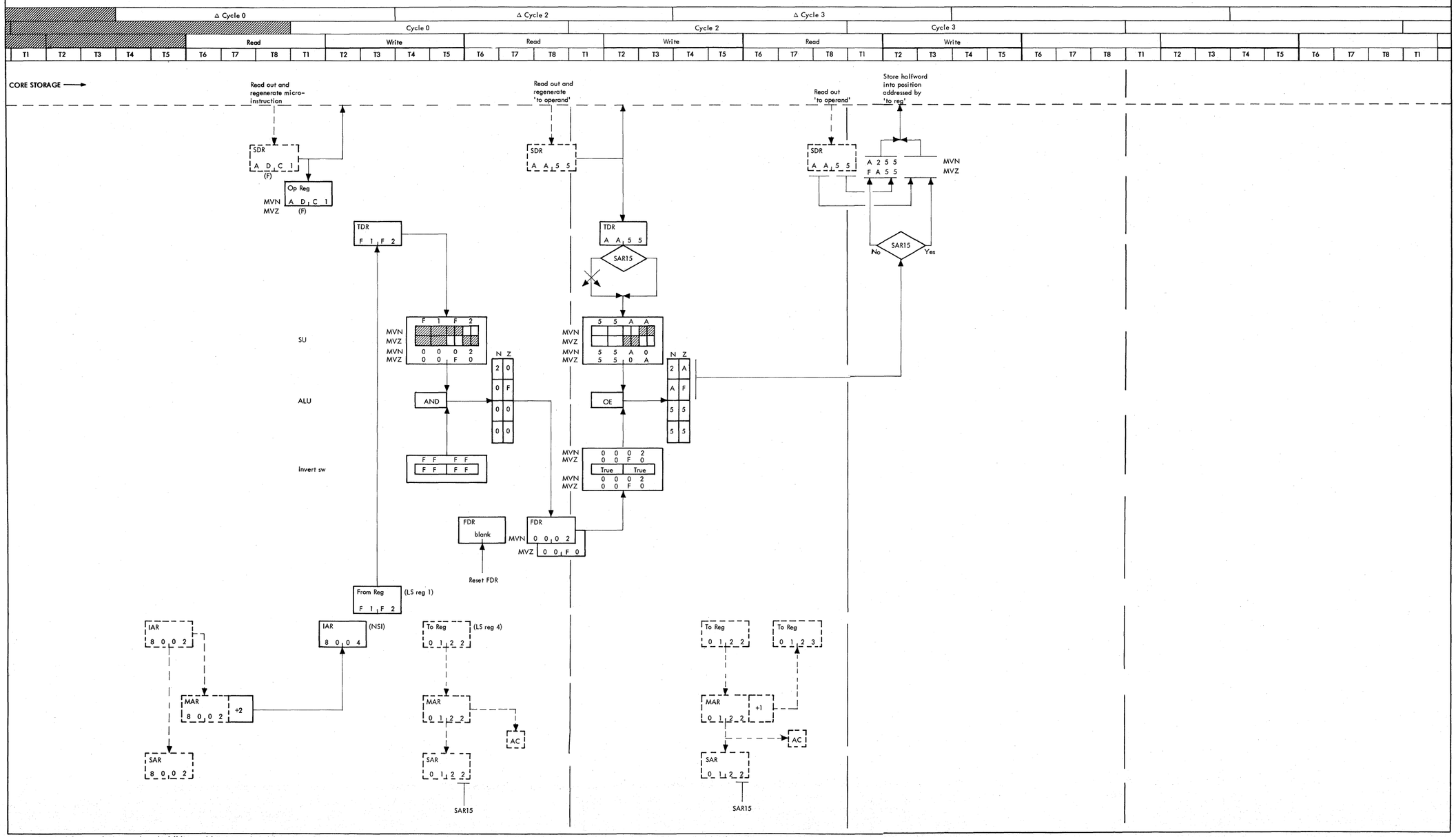
If on, the 'to addr' is checked that it is not outside customer area — XD

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
ADC1	MVN	4I,1,AC	BY(R4,AC,+1).4-7*=R1.12-15
AFC1	MVZ	4I,1,AC	BY(R4,AC,+1).0-3*=R1.8-11

Mnemonic
MVN
MVZ
Format
FF
Type
XD

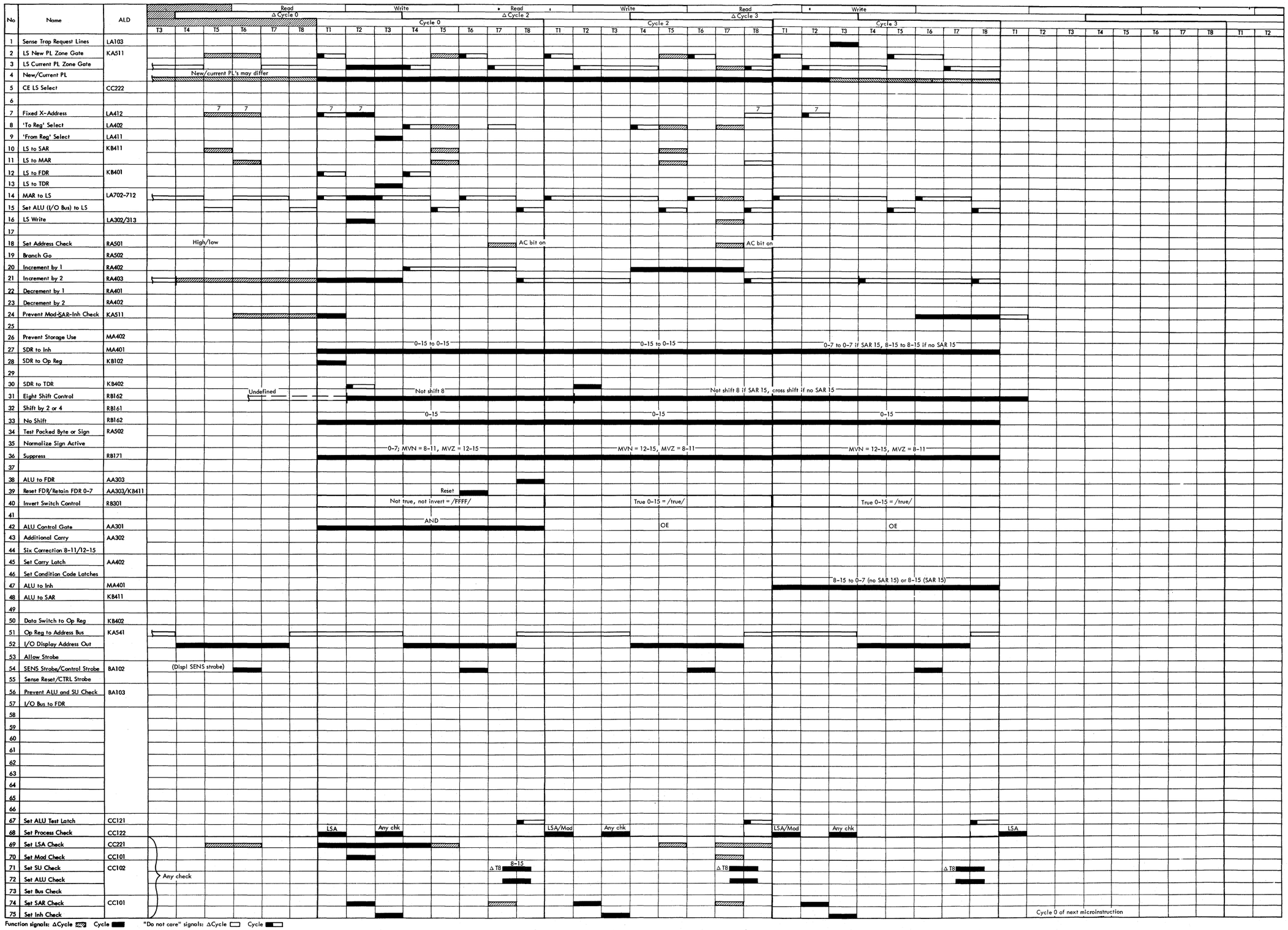
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59		
60		
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



Function signals: Δ Cycle ▨ Cycle ■ "Do not care" signals: Δ Cycle □ Cycle ▭

● Diagram 5-40. Move Numeric/Zone (XD) (Part 2 of 2) (03745A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

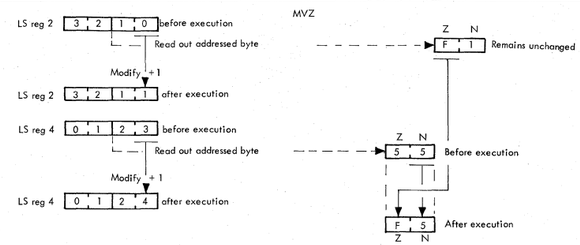
The numeric (zone) of the byte addressed by the 'from reg' is moved into the numeric (zone) of the byte addressed by the 'to reg'.

The 'from' byte and the zone (numeric) of the 'to' byte remain unchanged.

Both operand addresses are incremented by 1. If the AC bit (instruction bit 7) is on, an address check occurs when the 'from reg' or 'to reg' address is outside customer area.

The operation is performed in ALC mode when 'to reg' = 3 and 'from reg' = 5. LS register 1 contains the field length. The field length is the real number of numerics (zones) to be moved reduced by 1.

For ALC, the operand addresses are incremented by 1 every time one numeric (zone) has been moved.



Microinstruction Layout

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
Op Code							AC	To Reg				From Reg				
A		1	1	0		1						!				MVN
A		1	1	1		1						!				MVZ

If on, the 'from' and 'to' addr's are checked that they are not outside customer area — XX

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
ADCA	MVN	4I,2I,AC	BY(R4,AC,+1).4-7*=BY(R2,AC,+1).4-7
AFCA	MVZ	4I,2I,AC	BY(R4,AC,+1).0-3*=BY(R2,AC,+1).0-3
AFBD	MVZ	3I,5I,AC	BY(R3,AC,+1,UNTIL R1,LT,0).0-3*=BY(R5,AC,+1).0-3

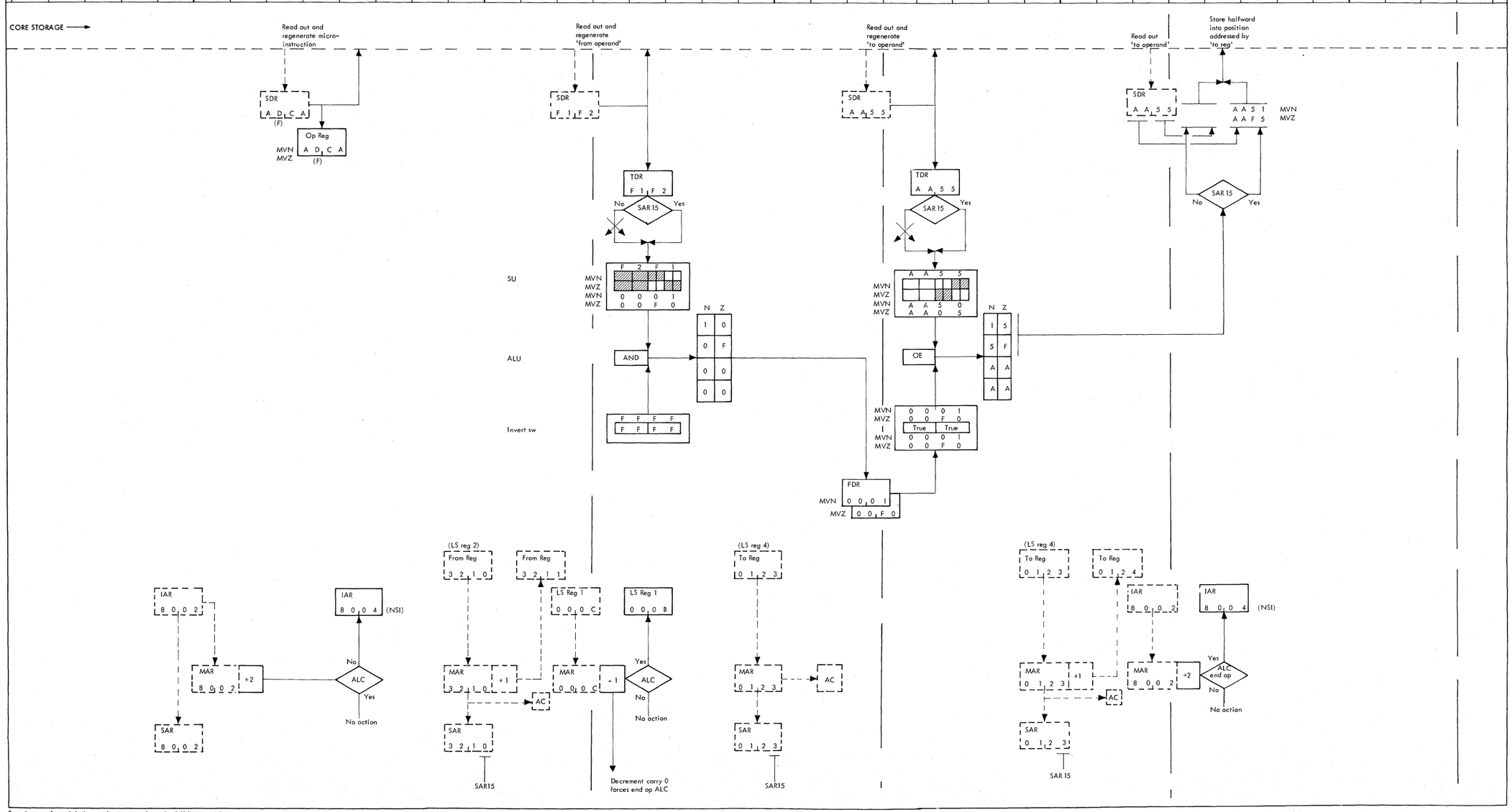
Mnemonic
MVN
MVZ
Format
FF
Type
XX (ALC)

Repeat Δ Cycle 1 - Δ Cycle 2 - Δ Cycle 3 — ALC end op — No / Yes → Δ Cycle 0

Δ Cycle 0	Δ Cycle 1	Δ Cycle 2	Δ Cycle 3
Cycle 0	Cycle 1	Cycle 2	Cycle 3
Read / Write	Read / Write	Read / Write	Read / Write
T1 T2 T3 T4 T5 T6 T7 T8 T1	T2 T3 T4 T5 T6 T7 T8 T1	T2 T3 T4 T5 T6 T7 T8 T1	T2 T3 T4 T5 T6 T7 T8 T1

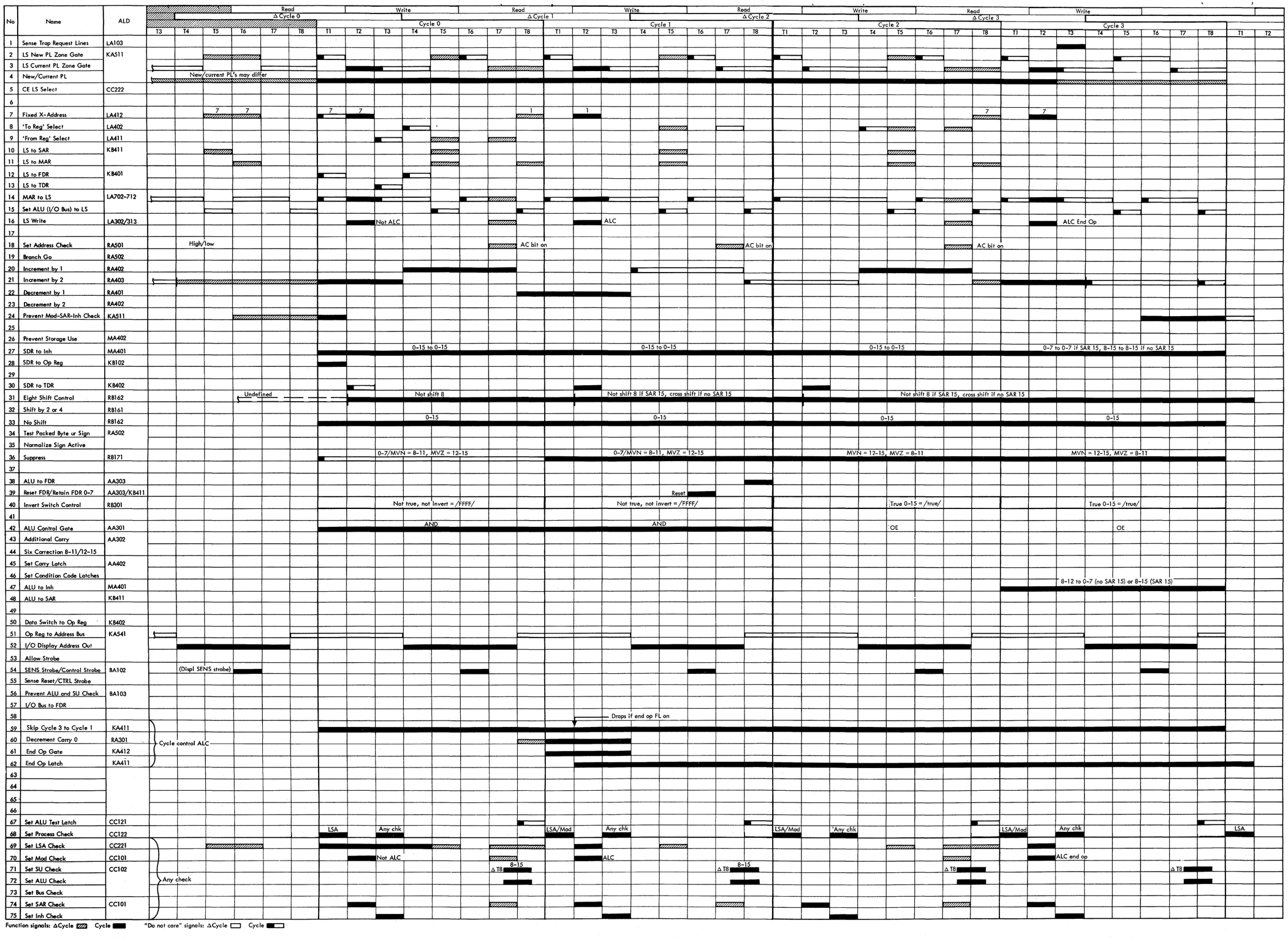
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59	Skip Cycle 3 to Cycle 1	KA411
60	Decrement Carry 0	RA301
61	End Op Gate	KA412
62	End Op Latch	KA411
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	

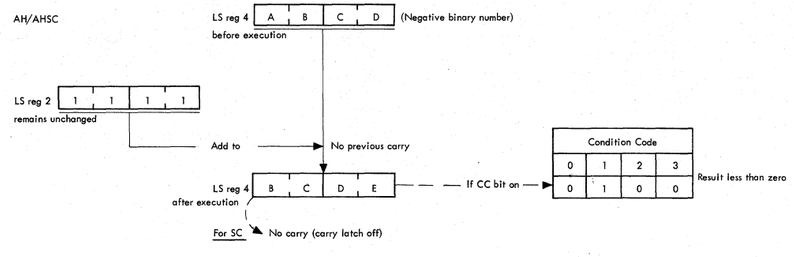


Function signals: Δ Cycle ▨ Cycle ■ "Do not care" signals: Δ Cycle □ Cycle ■

The 'from reg' is added to (or subtracted from) the 'to reg'. The result is set into 'to reg'. The 'from reg' remains unchanged. The condition code latches are set if the CC bit (instruction bit 6) is on.

For set carry (SC) instructions a carry out of the halfword turns on the carry latch, and a previous carry is implemented in the addition (or subtraction).

For SHSC a previous carry must be simulated by turning on the carry latch (aux carry latch). The carry latch can be turned on by a CTRL microinstruction. (ctrl /10/, bit 11).



Microinstruction Layout

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
Op Code						CC	AC	To Reg				From Reg				
B		0	0					0				0				AH
B		0	1					0				0				AHSC
B		1	0					0	4			0	0			SH
B		1	1					0				0				SHSC

Set condition code if on — DD

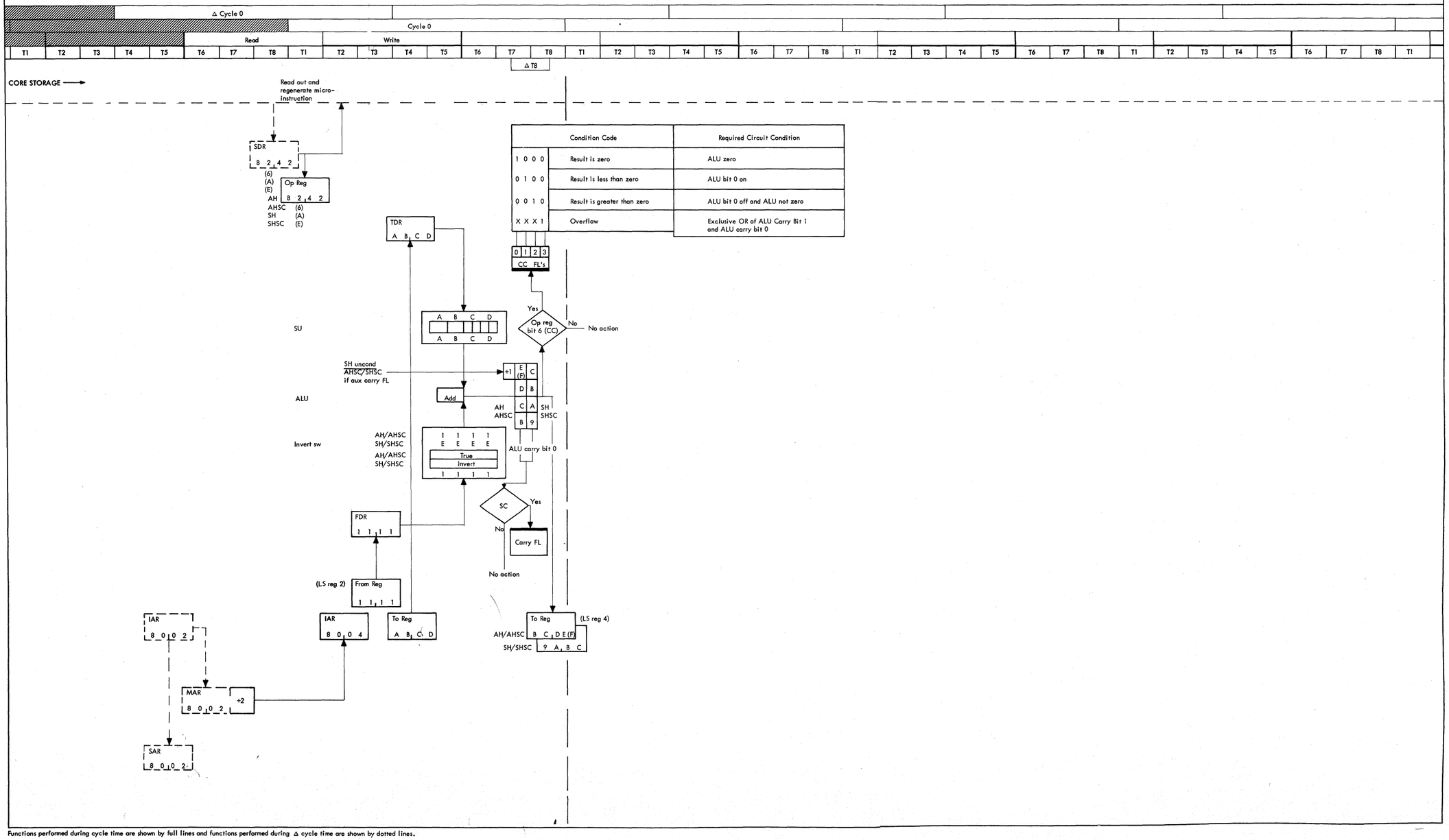
Ignored

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
B242	AH	4,2,CC	CC,R4+=R4+R2
B642	AHSC	4,2,CC	CC,C/R4+=R4+R2+C
BA42	SH	4,2,CC	CC,R4+=R4-R2
BE42	SHSC	4,2,CC	CC,C/R4+=R4-R2-NOT C

Mnemonic
AH
AHSC
SH
SHSC
Format
FF
Type
DD

Note: For "Do not care" functions refer to timing chart below.

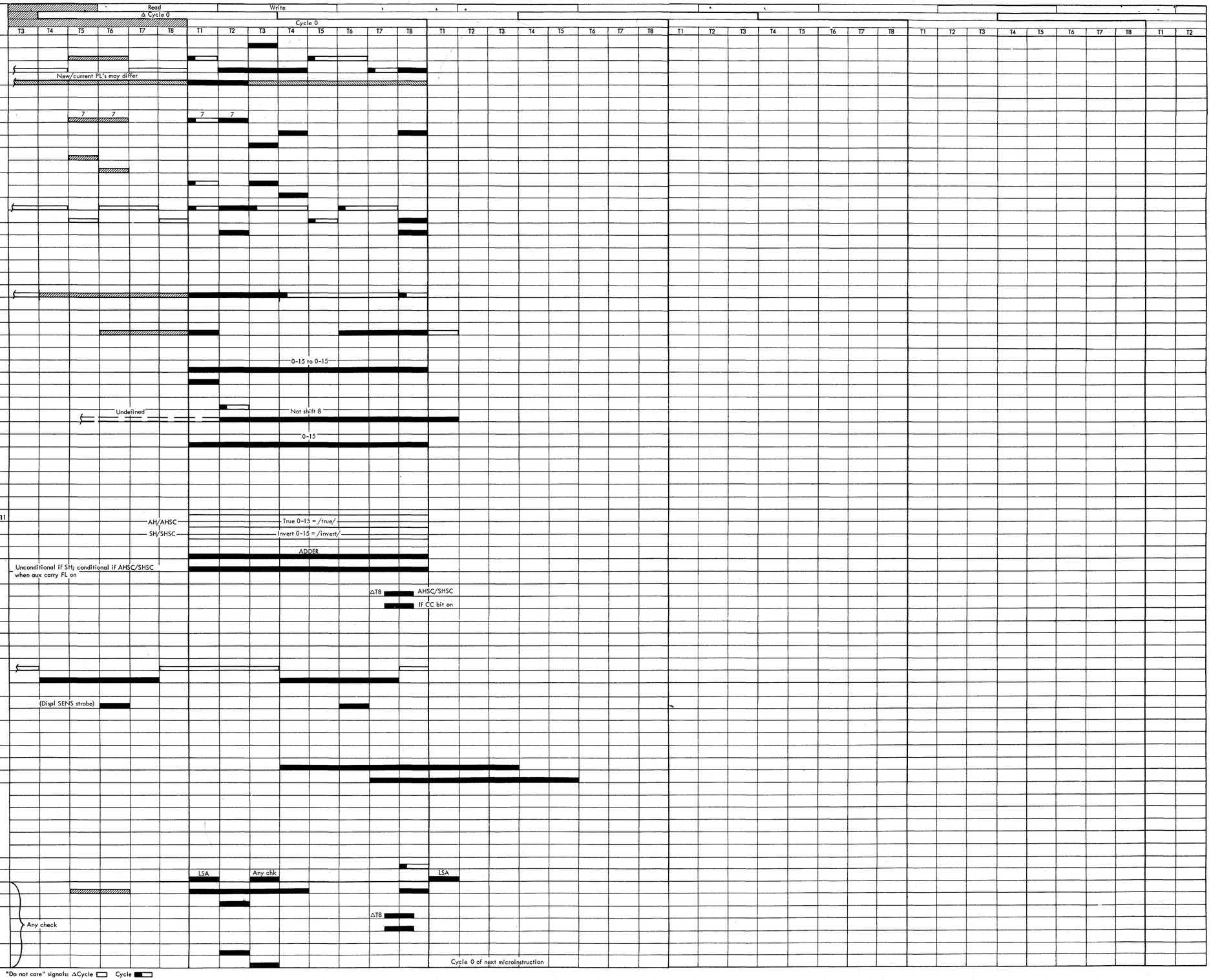
"Do not care" signals:
△Cycle
Cycle



Functions performed during cycle time are shown by full lines and functions performed during △ cycle time are shown by dotted lines.

Diagram 5-42. Add/Subtract Halfword, Add/Subtract Halfword and Set Carry (DD) (Part 1 of 2) (03747A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59	Set CC and Carry	AA411
60	Allow CC Setting Latch	AA412
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▬

Diagram 5-42. Add/Subtract Halfword, Add/Subtract Halfword and Set Carry (DD) (Part 2 of 2) (03747A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

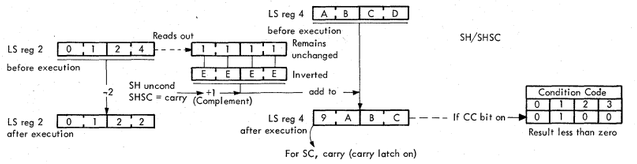
The halfword addressed by the 'from reg' is added to (or subtracted from) the 'to reg'. The result is set into 'to reg'. The 'from' halfword remains unchanged. The condition code latches are set if the CC bit (instruction bit 6) is on.

A previous carry (aux carry latch on) is implemented in the addition (subtraction).

For SHSC a previous carry must be simulated, if not already present, to obtain a valid two's complement of the 'from operand'. The carry latch can be turned on by a ctrl /10/, bit 11, as well as during arithmetical ALU operations.

For SC instructions a carry during addition (subtraction) turns on the carry latch.

The 'from reg' address is decremented by 2. If the AC bit (instruction bit 7) is on, an address check occurs when the 'from reg' address is outside customer area or not on halfword boundary.



Microinstruction Layout

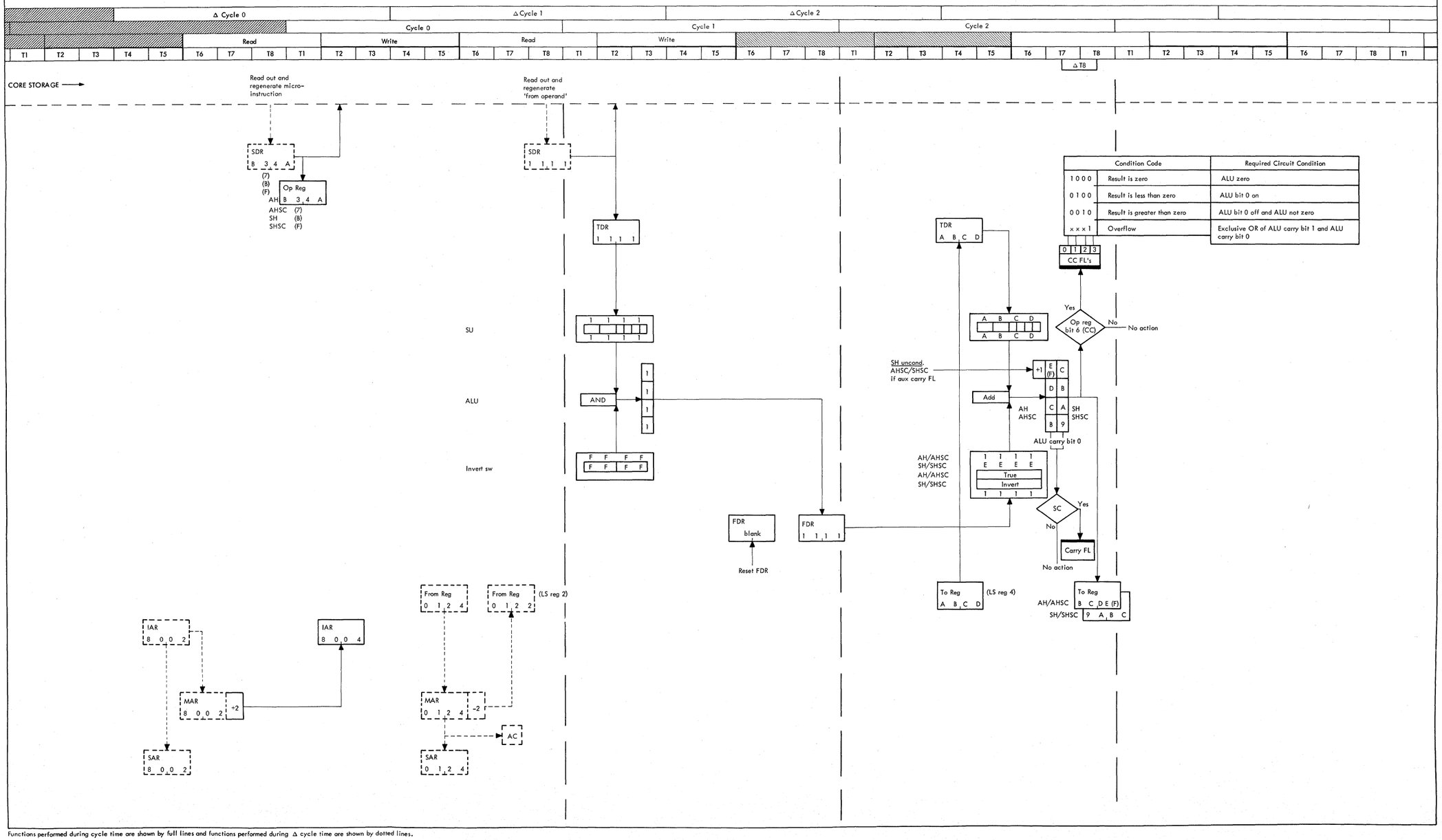
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
Op Code						CC	AC	To Reg				From Reg				
B		0	0					0				1				AH
B		0	1					0				1				AHSC
B		1	0					0				1				SH
B		1	1					0				1				SHSC

Set condition code if on
If on, the 'from addr' is checked that it is not outside customer area

DX

Mnemonic
AH
AHSC
SH
SHSC
Format
FF
Type
DX

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
B34A	AH	4,2I,CC,AC	CC,R4+=R4+HW(R2,AC,-2)
B74A	AHSC	4,2I,CC,AC	CC,C/R4+=R4+HW(R2,AC,-2)+C
BB4A	SH	4,2I,CC,AC	CC,R4+=R4-HW(R2,AC,-2)
BF4A	SHSC	4,2I,CC,AC	CC,C/R4+=R4-HW(R2,AC,-2)- NOT C



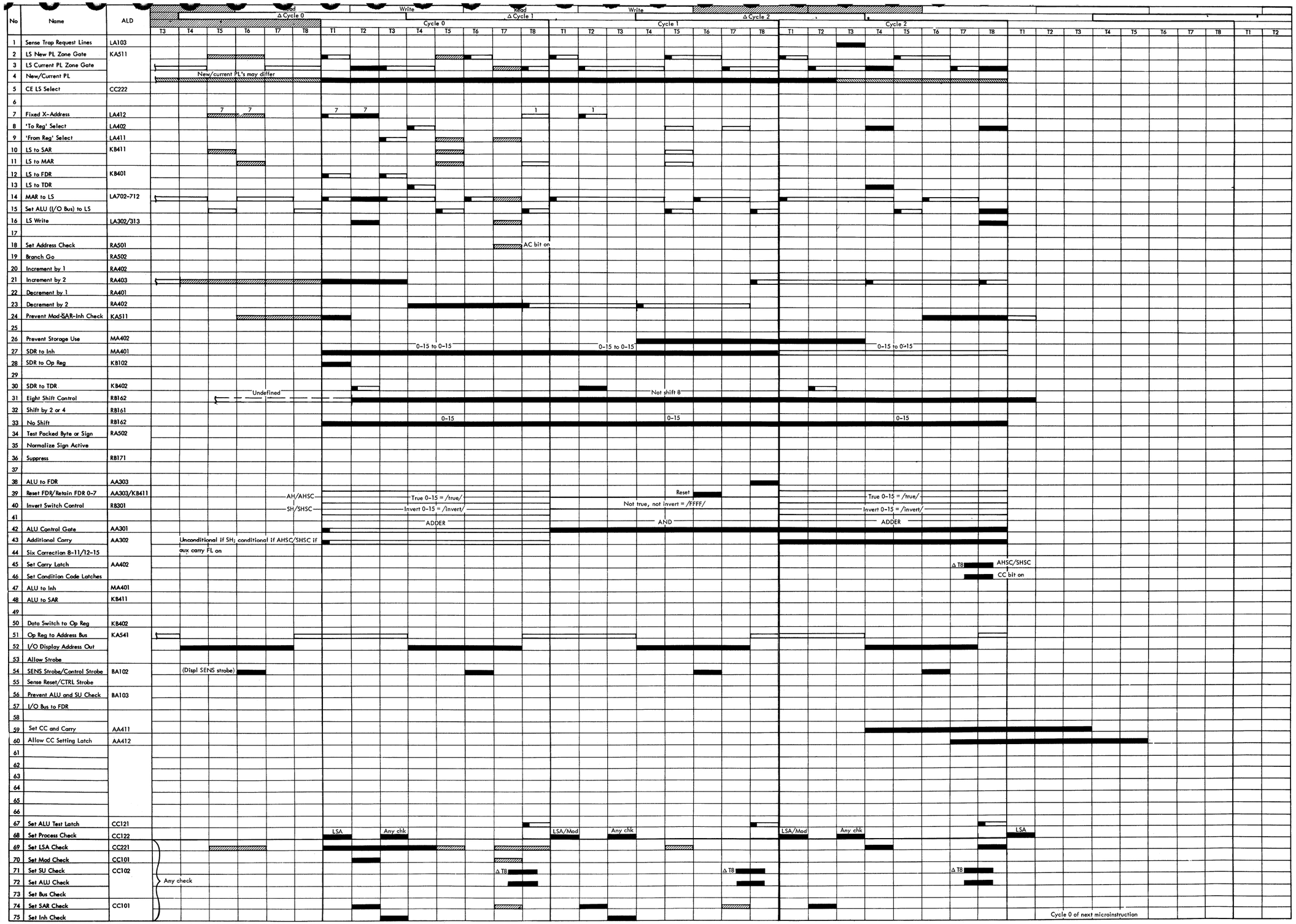
Condition Code	Required Circuit Condition
1 0 0 0	Result is zero	ALU zero
0 1 0 0	Result is less than zero	ALU bit 0 on
0 0 1 0	Result is greater than zero	ALU bit 0 off and ALU not zero
x x x 1	Overflow	Exclusive OR of ALU carry bit 1 and ALU carry bit 0

Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle

Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59	Set CC and Carry	AA411
60	Allow CC Setting Latch	AA412
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▭

● Diagram 5-43. Add/Subtract Halfword, Add/Subtract Halfword and Set Carry (DX) (Part 2 of 2) (03748A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

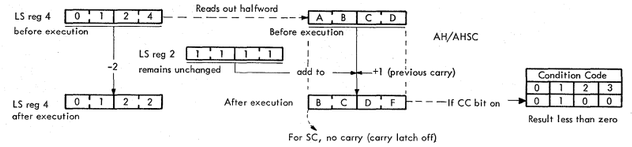
The 'from reg' is added to (subtracted from) the halfword addressed by the 'to reg'. The result is set into the halfword addressed by the 'to reg'. The 'from reg' remains unchanged. The condition code latches are set if the CC bit (instruction bit 6) is on.

A previous carry (aux carry latch on) is implemented in the addition (subtraction).

For SHSC a previous carry must be simulated, if not already present, to obtain a valid two's complement of the 'from operand'. The carry latch can be turned on by a ctrl /10/, bit 11, as well as during arithmetical ALU operations.

For SC instructions, a carry during addition (subtraction) of the two halfwords turns on the carry latch.

The 'to reg' address is decremented by 2. If the AC bit (instruction bit 7) is on, an address check occurs when the 'to reg' address is outside customer area or not on halfword boundary.



Microinstruction Layout

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
Op Code						CC	AC	To Reg				From Reg				
B		0	0					1				0				AH
B		0	1					1				0				AHSC
B		1	0					1				0				SH
B		1	1					1				0				SHSC

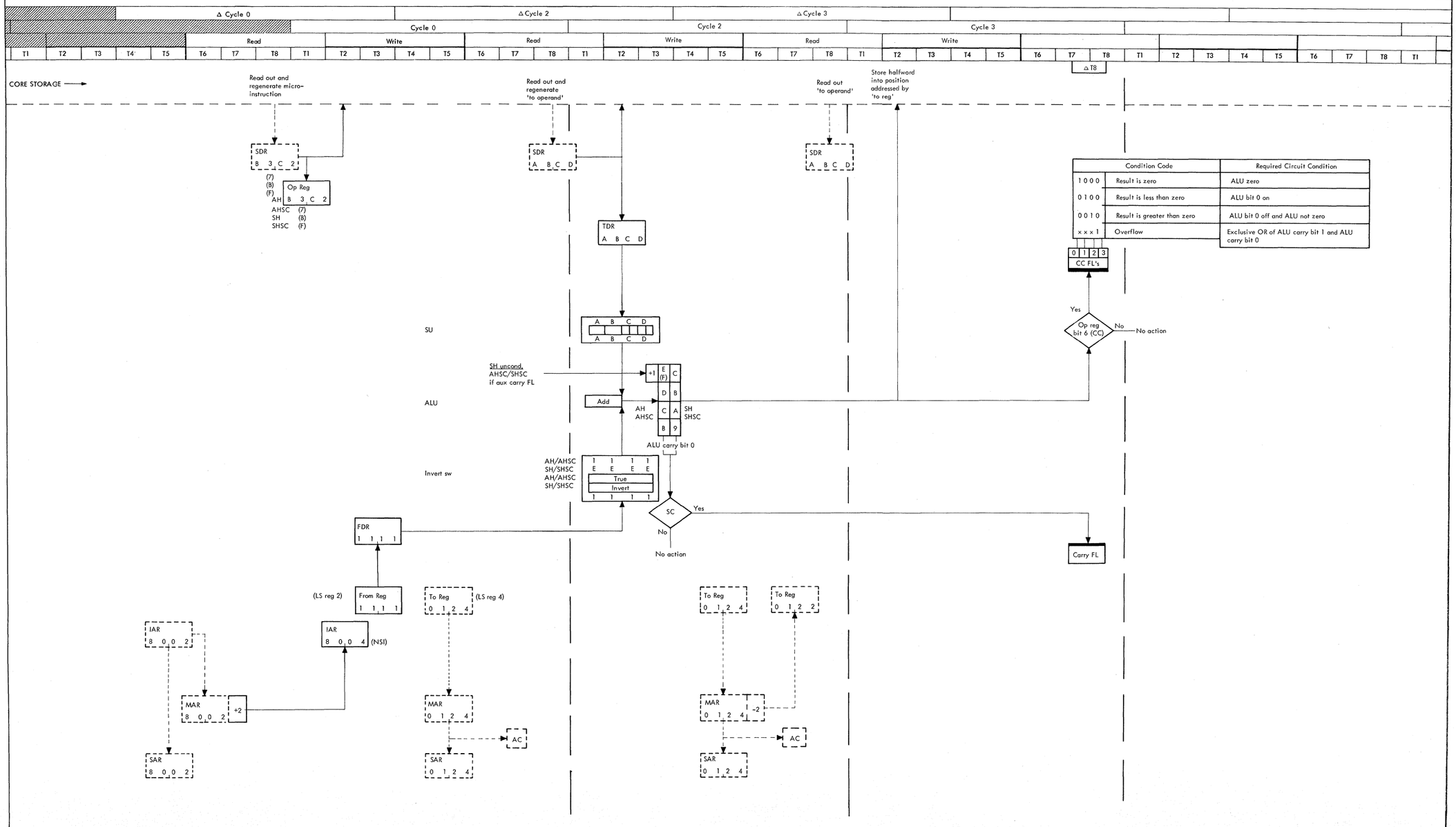
Set condition code if on
If on, the 'to addr' is checked that it is not outside customer area
XD

Mnemonic
AH
AHSC
SH
SHSC
Format
FF
Type
XD

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
B3C2	AH	4I,2,CC,AC	CC,HW(R4,AC)*=HW(R4,-2)+R2
B7C2	AHSC	4I,2,CC,AC	CC,C/HW(R4,AC)*=HW(R4,-2)+R2+C
BBC2	SH	4I,2,CC,AC	CC,HW(R4,AC)*=HW(R4-2)-R2
BFC2	SHSC	4I,2,CC,AC	CC,C/HW(R4,AC)*=HW(R4,-2)-R2-NOT C

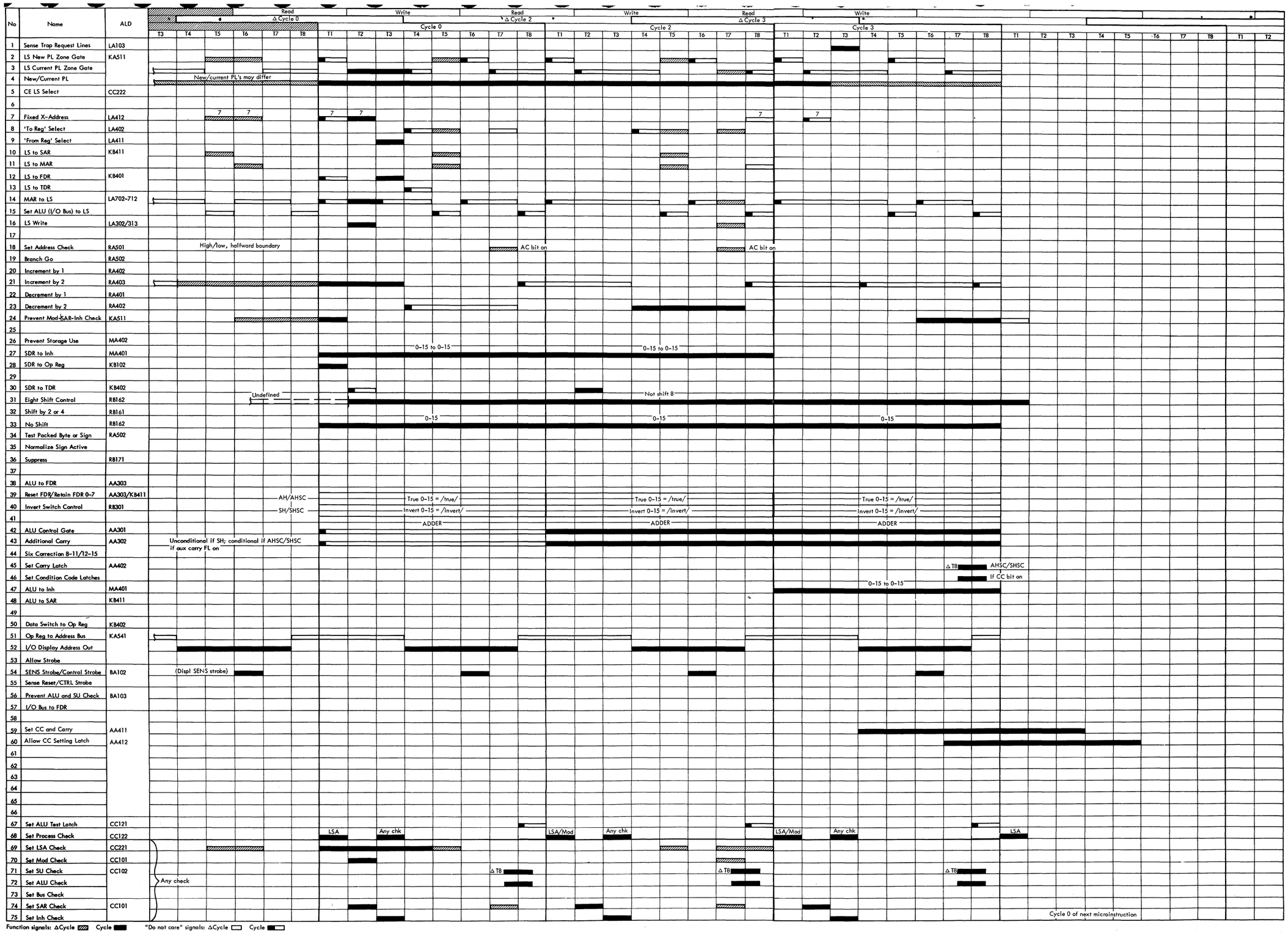
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59	Set CC and Carry	AA411
60	Allow CC Setting Latch	AA412
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▭

● Diagram 5-44. Add/Subtract Halfword, Add/Subtract Halfword and Set Carry (XD) (Part 2 of 2) (03749A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

The halfword addressed by the 'from reg' is added to (subtracted from) the halfword addressed by the 'to reg'. The result is set into the halfword addressed by the 'to reg'. The 'from' halfword remains unchanged.

The condition code latches are set if the CC bit (instruction bit 6) is on.

A previous carry (aux carry latch on) is implemented in the addition (subtraction).

For SHSC a previous carry must be simulated, if not already present, to obtain a valid two's complement of the 'from operand'. The carry latch can be turned on by a ctrl /10/, bit 11, as well as during arithmetical ALU operations.

For SC instructions a carry during addition (subtraction) of the two halfwords turns on the carry latch.

Both operand addresses are decremented by 2. If the AC bit (instruction bit 7) is on, an address check occurs when the 'from reg' or 'to reg' address is outside customer area or not on halfword boundary.

The operation is performed in ALC mode when 'to reg' = 3 and 'from reg' = 5; LS register 1 contains the field length. The field length must reflect the number of bytes to be operated (always an even number) reduced by 2.

For ALC, the operand addresses are updated by -2 every time a halfword is added (subtracted).

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
B3CA	AH	4I,2I,CC,AC	CC,HW(R4,AC)+=HW(R4,-2)+HW(R2,AC,-2)
B7CA	AHSC	4I,2I,CC,AC	CC,C/HW(R4,AC)+=HW(R4,-2)+HW(R2,AC,-2)+C
BBCA	SH	4I,2I,CC,AC	CC,HW(R4,AC)+=HW(R4,-2)-HW(R2,AC,-2)
BFCA	SHSC	4I,2I,CC,AC	CC,C/HW(R4,AC)+=HW(R4,-2)-HW(R2,AC,-2)-NOT C
B7BD	AHSC	3I,5I,CC,AC	CC,C/HW(R3,AC)+=HW(R3,-2, UNTIL R1,LT,0)+HW (R2,AC,-2)+C

Miscroinstruction Layout

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
Op Code				CC	AC	To Reg				From Reg						
B		0	0			1				1						AH
B		0	1			1				1						AHSC
B		1	0			1				1						SH
B		1	1			1				1						SHSC

Set condition code if on

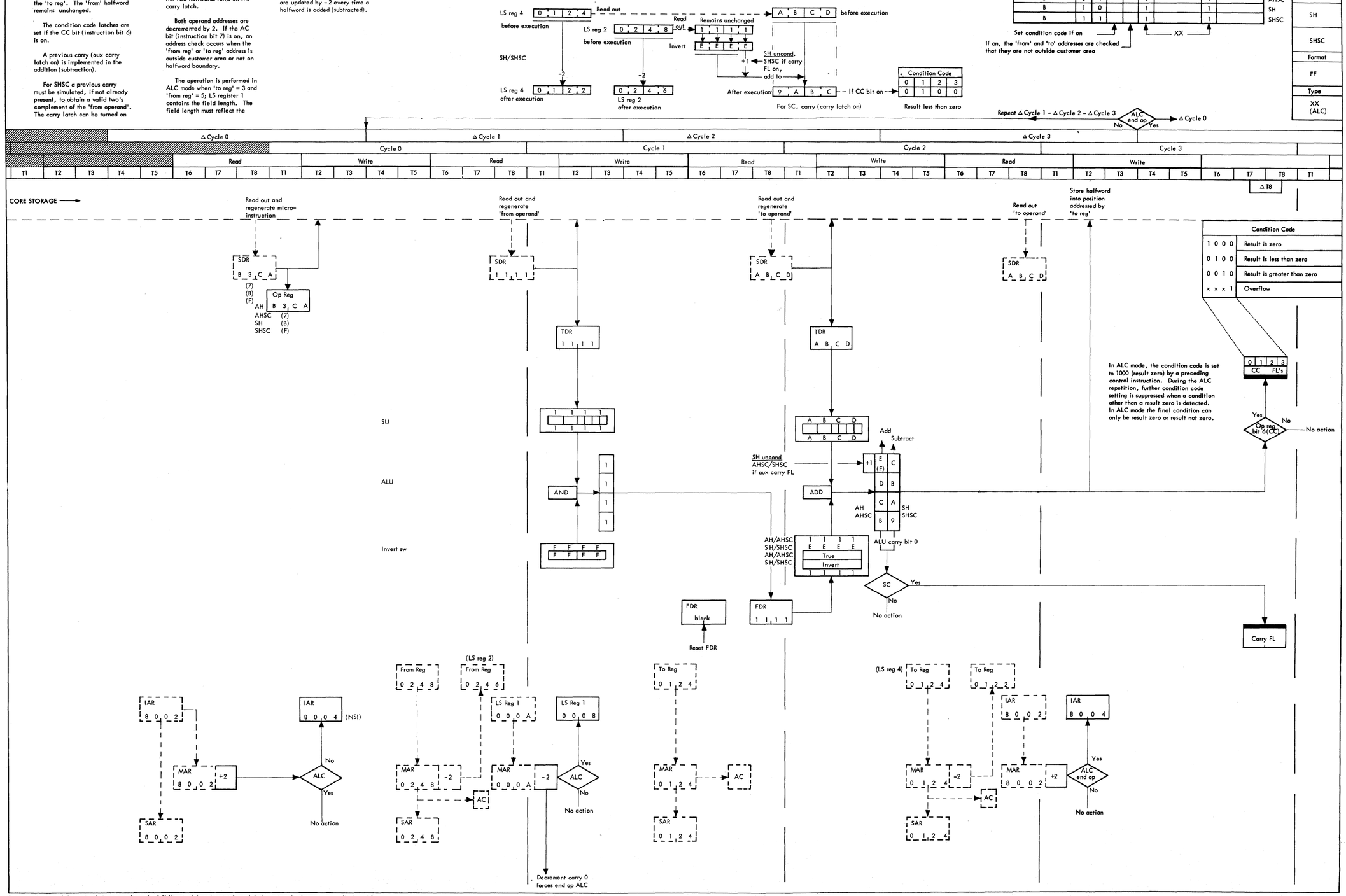
If on, the 'from' and 'to' addresses are checked that they are not outside customer area

XX

Mnemonic
AH
AHSC
SH
SHSC
Format
FF
Type
XX (ALC)

Note: For "Do not care" functions refer to timing chart below.

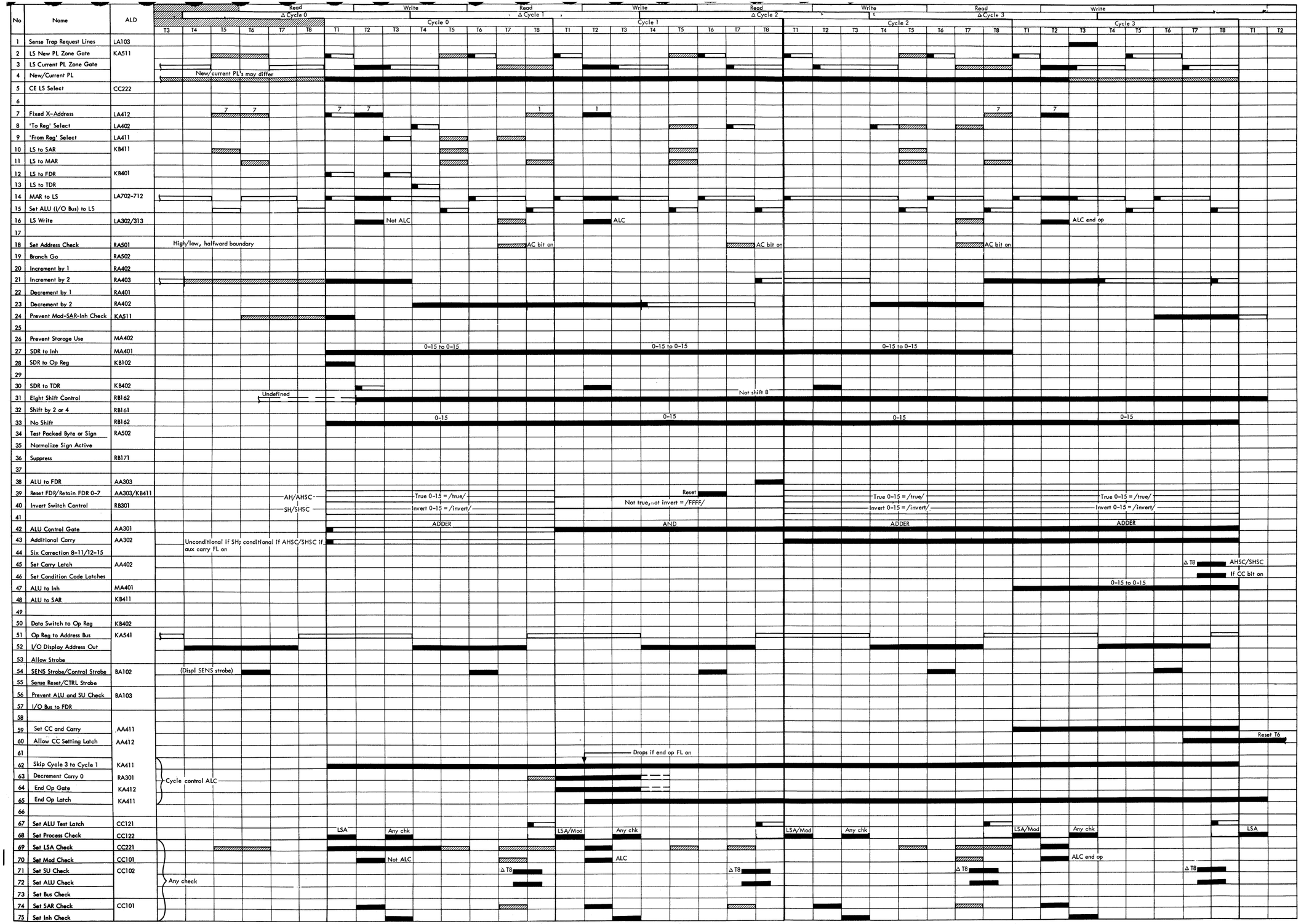
"Do not care" signals:
ΔCycle
Cycle



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

Diagram 5-45. Add/Subtract Halfword, Add/Subtract Halfword and Set Carry (XX, ALC) (Part 1 of 2) (03750A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59	Set CC and Carry	AA411
60	Allow CC Setting Latch	AA412
61		
62	Skip Cycle 3 to Cycle 1	KA411
63	Decrement Carry 0	RA301
64	End Op Gate	KA412
65	End Op Latch	KA411
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	

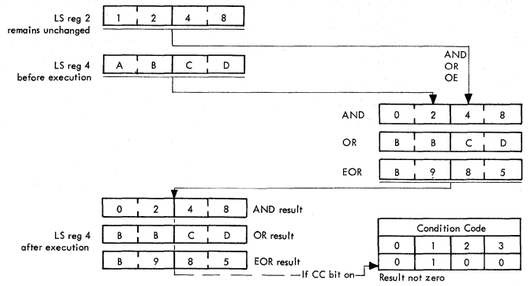


Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▭

● Diagram 5-45. Add/Subtract Halfword, Add/Subtract Halfword and Set Carry (XX, ALC) (Part 2 of 2) (03750A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

The 'from reg' is ANDed, ORed, or exclusive ORed with the 'to reg'. The result is set into 'to reg'. The 'from reg' remains unchanged. The condition code latches are set if the CC bit (instruction bit 6) is on.

The address check is ignored.



Microinstruction Layout

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
Op Code						CC	AC	To Reg				From Reg				
C			0	0				0				0				AND
C			0	1				0				0				OR
C			1	0				0				0				EOR

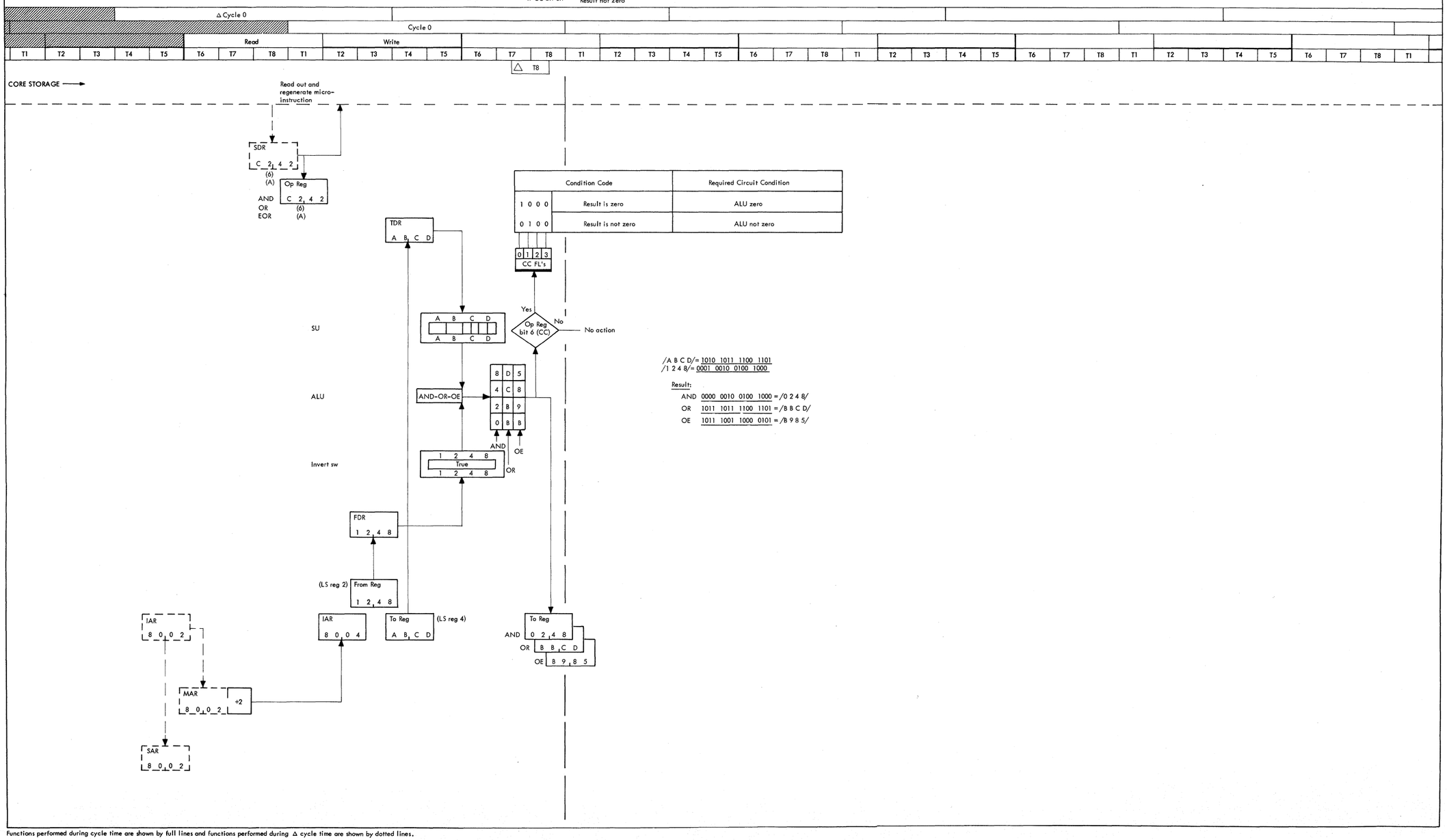
Set condition code if on
Ignored
DD

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
C242	AND	4,2,CC	CC,R4←R4,A,R2
C642	OR	4,2,CC	CC,R4←R4,OR,R2
CA42	EOR	4,2,CC	CC,R4←R4,OE,R2

Mnemonic
AND
OR
EOR
Format
FF
Type
DD

Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
- △Cycle
- Cycle

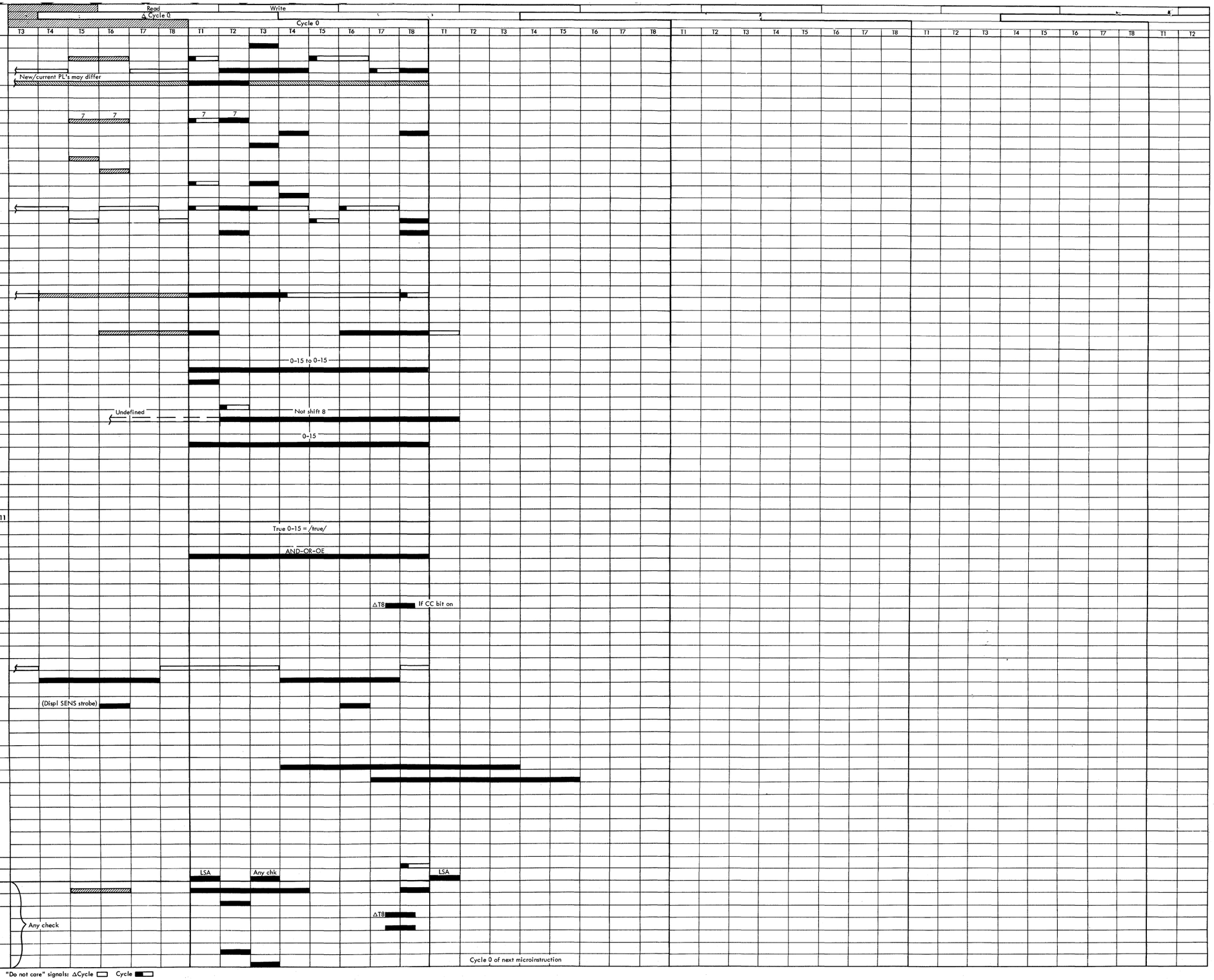


/A B C D/= 1010 1011 1100 1101
/1 2 4 8/= 0001 0010 0100 1000

Result:
AND 0000 0010 0100 1000 = /0 2 4 8/
OR 1011 1011 1100 1101 = /B B C D/
OE 1011 1001 1000 0101 = /B 9 8 5/

Functions performed during cycle time are shown by full lines and functions performed during △ cycle time are shown by dotted lines.

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59	Set CC and Carry	AA411
60	Allow CC Setting Latch	AA412
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



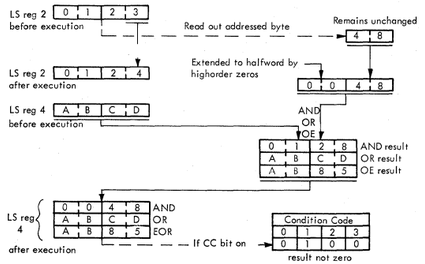
Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▭

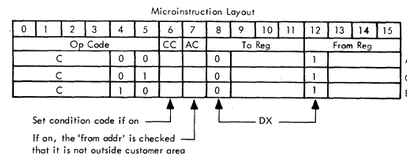
Diagram 5-46. AND-OR-Exclusive OR Byte or Halfword (DD) (Part 2 of 2) (03751A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

The byte addressed by the 'from reg' is ANDed, ORed, or exclusive ORed with the halfword in 'to reg'. The 'from' byte is extended to a halfword by high-order zeros. The result is set into 'to reg'. The from byte remains unchanged.

The condition code latches are set if the CC bit (instruction bit 6) is on.

The 'from reg' address is incremented by 1. If the AC bit (instruction bit 7) is on, an address check occurs when the from reg address is outside customer area.



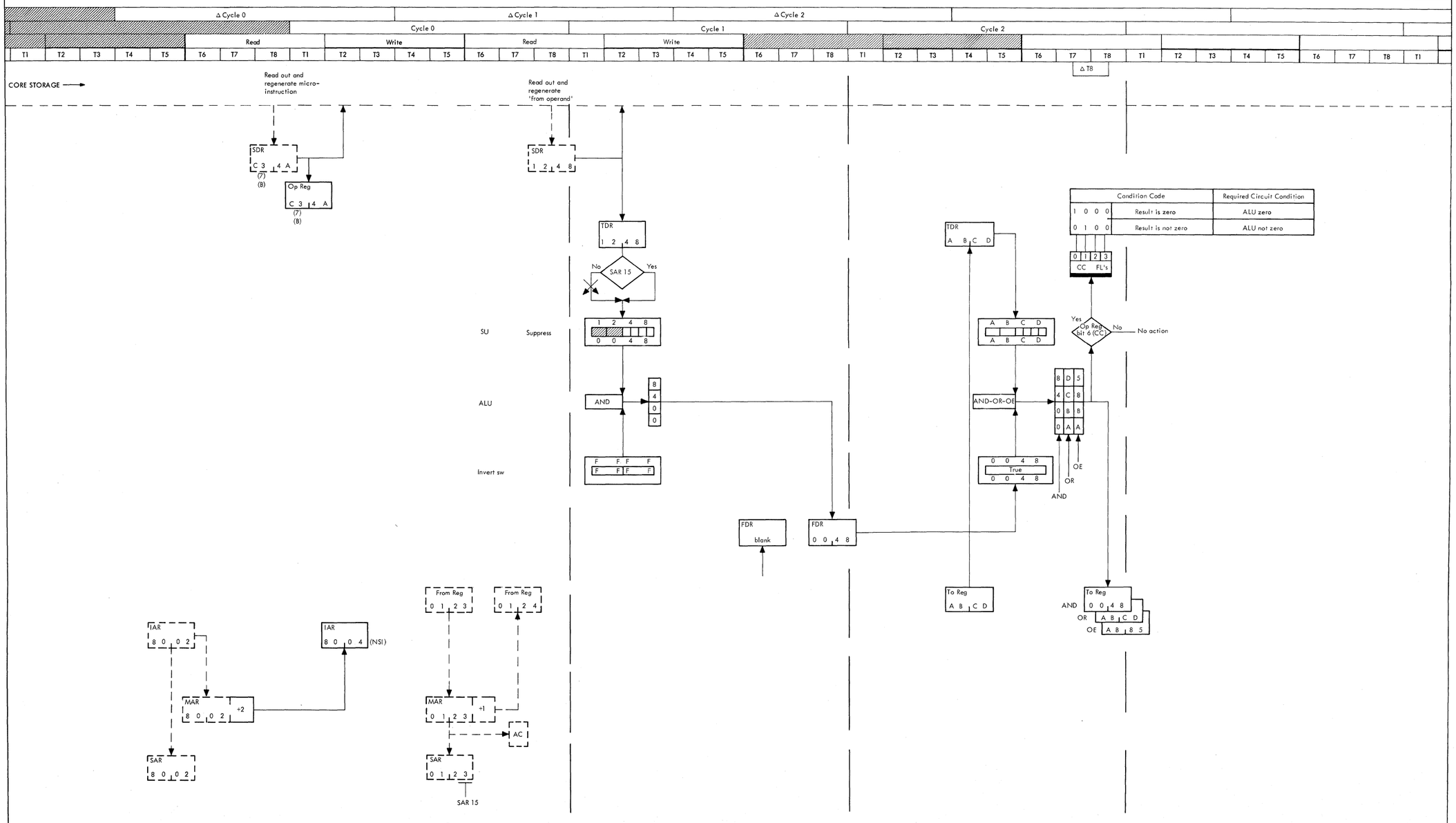


Mnemonic
AND
OR
EOR
Format
FF
Type
DX

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
C34A	AND	4,2I,CC,AC	CC,R4*=R4,A,'00'/BY(R2,AC,+1)
C74A	OR	4,2I,CC,AC	CC,R4*=R4,OR,'00'/BY(R2,AC,+1)
CB4A	EOR	4,2I,CC,AC	CC,R4*=R4,OE,'00'/BY(R2,AC,+1)

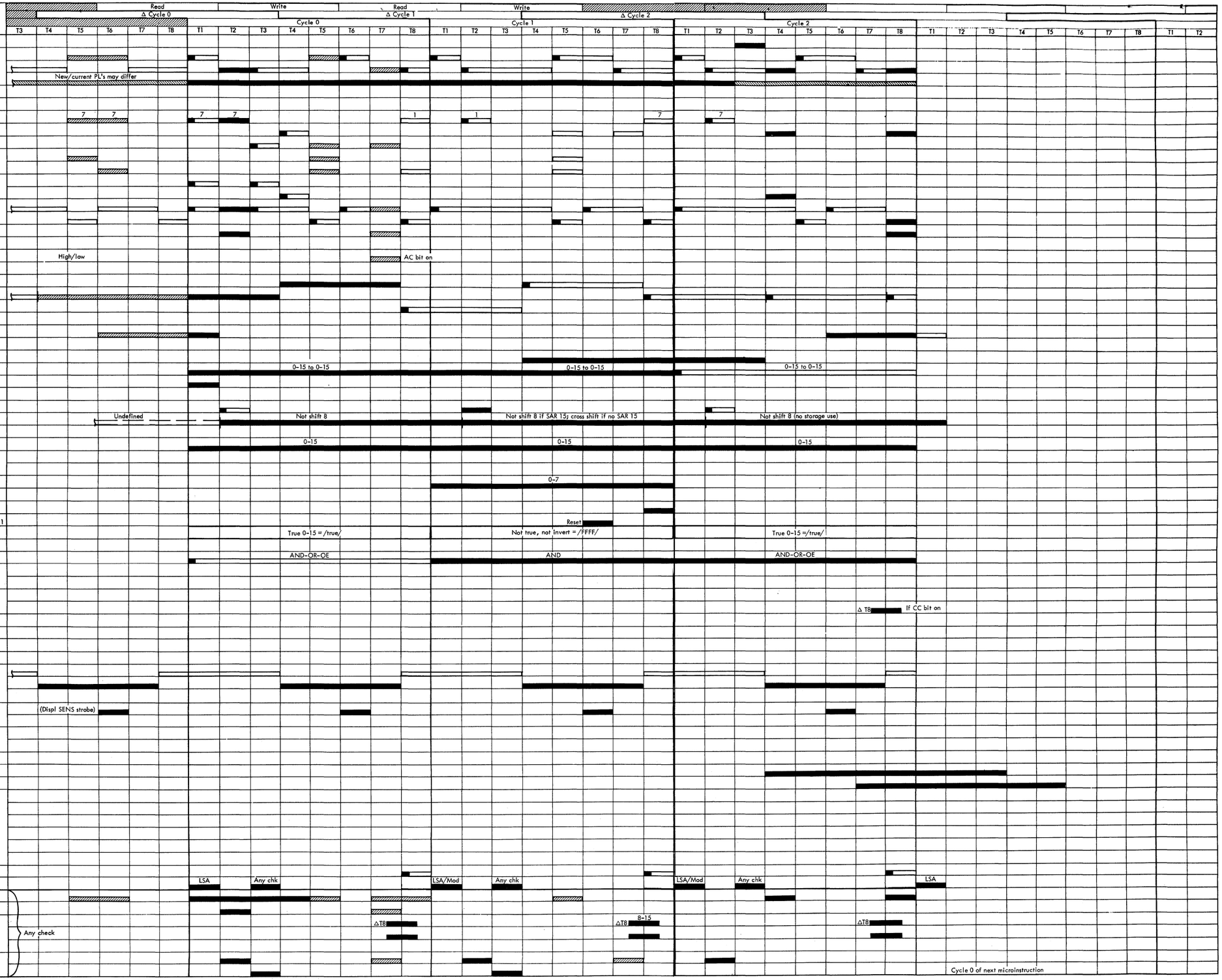
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59	Set CC and Carry	AA411
60	Allow CC Setting Latch	AA412
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	

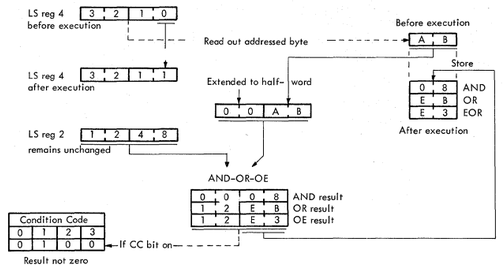


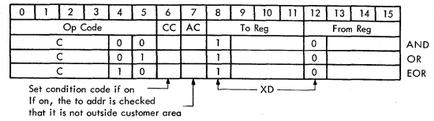
Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▭

The halfword in the from reg is ANDed, ORed, or exclusive ORed with the byte addressed by the 'to reg'. The 'to' byte is extended to a halfword by high-order zeros. The low-order result byte is set into the byte addressed by the 'to reg'. The 'from reg' remains unchanged.

The condition code latches are set according to the halfword result if the CC bit (instruction bit 6) is on.

The 'to reg' address is incremented by 1. If the AC bit (instruction bit 7) is on, an address check occurs when the 'to reg' address is outside customer area.



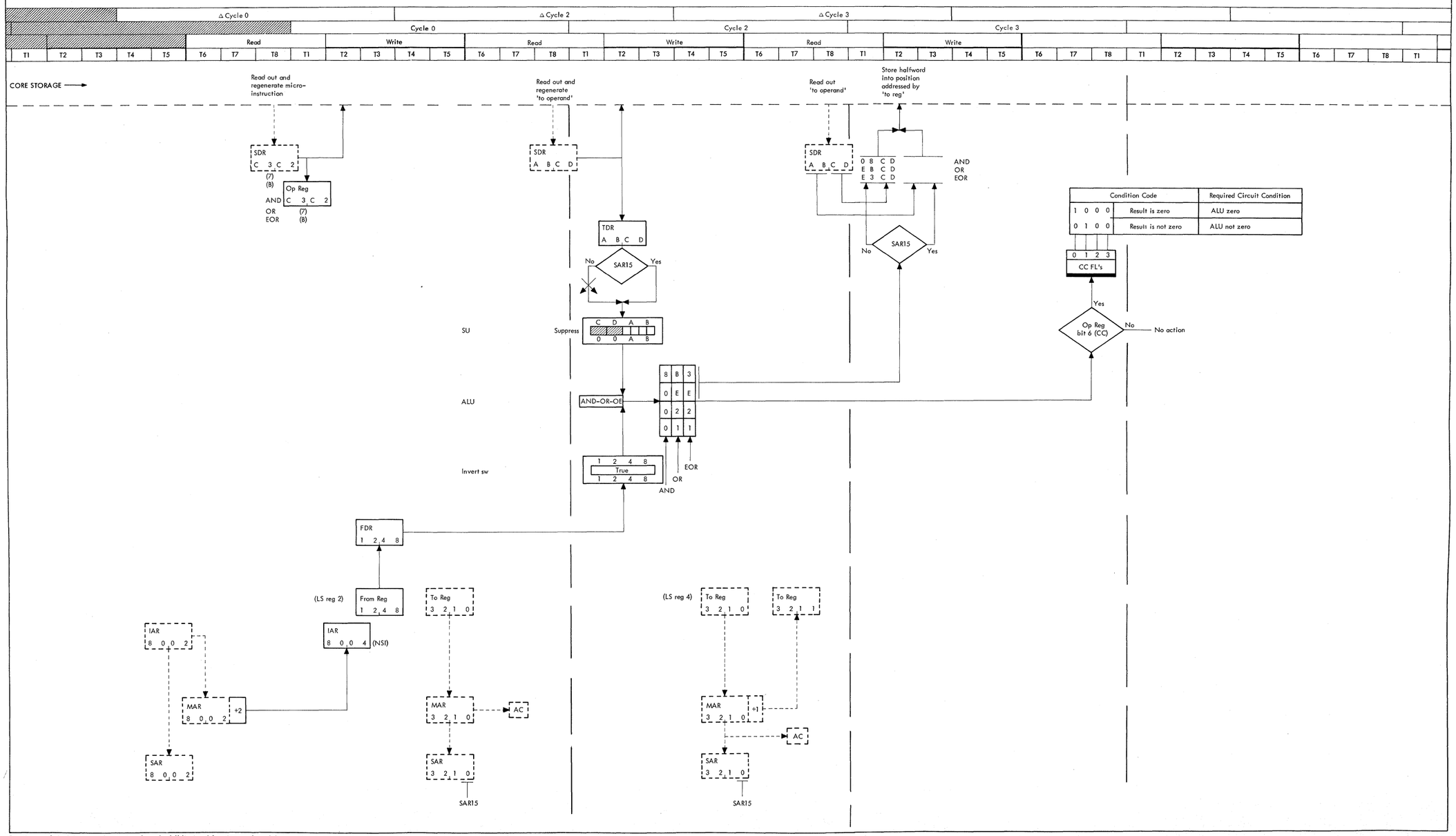


Mnemonic
AND
OR
EOR
Format
FF
Type
XD

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
C3C2	AND	4I,2,CC,AC	CC,BY(R4,AC)*=BY(R4,+1),A,R2.8-15
C7C2	OR	4I,2,CC,AC	CC,BY(R4,AC)*=BY(R4,+1),OR,R2.8-15
CBC2	EOR	4I,2,CC,AC	CC,BY(R4,AC)*=BY(R4,+1),OE,R2.8-15

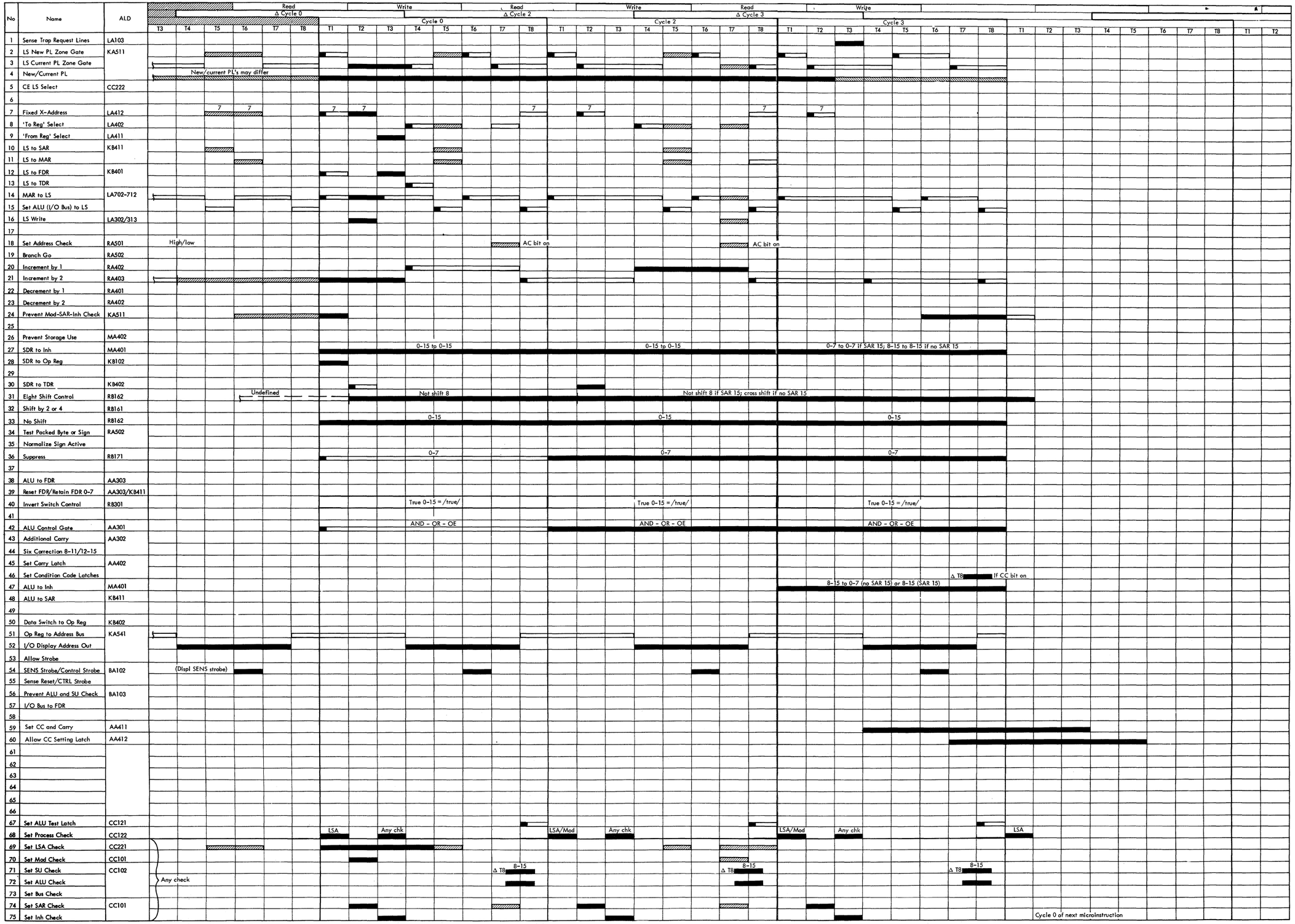
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
- △Cycle
- Cycle



Functions performed during cycle time are shown by full lines and functions performed during △ cycle time are shown by dotted lines.

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59	Set CC and Carry	AA411
60	Allow CC Setting Latch	AA412
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▭

● Diagram 5-48. AND-OR-Exclusive OR Byte or Halfword (XD) (Part 2 of 2) (03753A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

The byte addressed by the 'from reg' is ANDed, ORed, or exclusive ORed with the byte addressed by the 'to reg'. The result is set into the byte addressed by the 'to reg'. The 'from' byte remains unchanged.

The condition code latches are set, according to the result, if the CC bit (instruction bit 6) is on. Both operand addresses are incremented by 1.

If the AC bit (instruction bit 7) is on, an address check occurs when the 'to reg' or 'from reg' address is outside customer area.

The operation is performed in ALC mode when 'to reg' = 3 and 'from reg' = 5; LS register 1 contains the field length. The field length is the real number of bytes to be ANDed, ORed, or exclusive ORed reduced by 1. The operand addresses are incremented by 1 every time a byte has been operated.

LS reg 2 before execution: 0 1 2 3 → LS reg 2 after execution: 0 1 2 4 (+1)

LS reg 4 before execution: 3 2 1 0 → LS reg 4 after execution: 3 2 1 1 (+1)

Read out addressed byte → Remains unchanged: 4 8

Read out addressed byte: Before execution: A B

Store: AND / OR / EOR: 0 8 / E 8 / E 3 — after execution

AND-OR-OE: 0 8 AND result; E 8 OR result; E 3 OE result

If CC bit on → Condition Code: 0 1 2 3 / 0 1 0 0 — Result not zero

Microinstruction Layout

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Op Code						CC	AC	To Reg				From Reg			
C			0	0				1				1			AND
C			0	1				1				1			OR
C			1	0				1				1			EOR

Set condition code if on — XX

If on, the 'from' and 'to' addr's are checked that they are not outside customer area

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD GEB 0-1046-XXX
C3CA	AND	4I,2I,GG,AC	GG,BY(R4,AC)=BY(R4,+1),A,BY(R2,AC,+1)
C7CA	OR	4I,2I,GG,AC	GG,BY(R4,AC)=BY(R4,+1),OR,BY(R2,AC,+1)
CBCA	EOR	4I,2I,GG,AC	GG,BY(R4,AC)=BY(R4,+1),OE,BY(R2,AC,+1)
C3BD	AND	3I,5I,GG,AC	GG,BY(R3,AC,UNTIL R1,LT,0)=BY(R3,+1),A,BY(R5,AC,+1)

Mnemonic
AND
OR
EOR
Format
FF
Type
XX (ALC)

Repeat Δ Cycle 1 - Δ Cycle 2 - Δ Cycle 3 — No: ALC end op — Yes: Δ Cycle 0

Δ Cycle 0	Δ Cycle 1	Δ Cycle 2	Δ Cycle 3
Cycle 0	Cycle 1	Cycle 2	Cycle 3
Read / Write	Read / Write	Read / Write	Read / Write
T1 T2 T3 T4 T5 T6 T7 T8 T1	T2 T3 T4 T5 T6 T7 T8 T1	T2 T3 T4 T5 T6 T7 T8 T1	T2 T3 T4 T5 T6 T7 T8 T1

Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle

CORE STORAGE

Read out and regenerate micro-instruction

SDR C 3 C A (7) (8)

Op Reg C 3 C A (7) (8)

AND / OR / EOR

Read out and regenerate 'from operand'

SDR 1 2 4 8

TDR 1 2 4 8 — SAR 15: No / Yes

SU: 1 2 4 8 / 0 0 4 8 — Suppress

ALU: AND — 8 4 0 0

Invert sw: F F F F / F F F F

Read out and regenerate 'to operand'

SDR A B C D

TDR A B C D — SAR 15: No / Yes

Suppress: C D A B / 0 0 A B

AND-OR-OE

FDR blank — Reset FDR

FDR 0 0 4 8

0 0 4 8 True / 0 0 4 8

Read out 'to operand'

SDR A B C D

AND: 0 8 C D

OR: E B C D

EOR: E 3 C D

SAR 15: No / Yes

Store halfword into position addressed by 'to reg'

8 B 3 / 0 E E / 0 0 0 / 0 0 0

/AB/ = 1010 1011

/48/ = 0100 1000

RESULT:

AND 0000 1000 = /08/

OR 1110 1011 = /EB/

OE 1110 0011 = /E3/

Condition Code

1 0 0 0 Result is zero

0 1 0 0 Result is not zero

0 1 2 3 CC FL's

Op reg bit 6 (CC): Yes / No — No action

For condition code setting in ALC mode, the condition code latches should be set to 1000 (result zero) by a preceding CTRL instruction. Further condition code setting is suppressed when a condition code other than zero is detected. In ALC mode the condition code can only be result zero or not zero.

IAR 8 0 0 2 → MAR 8 0 0 2 +2 → IAR 8 0 0 4

ALC: No / Yes — No action

SAR 8 0 0 2

(LS reg 2) From Reg 0 1 2 3 → MAR 0 1 2 3 +1 → AC

From Reg 0 1 2 4

LS Reg 1 0 0 0 A → LS Reg 1 0 0 0 9

LS Reg 1 -1 — ALC: Yes / No — No action

Decrement carry 0 forces end op ALC

SAR 0 1 2 3 — SAR 15

To Reg 3 2 1 0 (LS reg 4) → MAR 3 2 1 0 → AC

SAR 3 2 1 0 — SAR 15

To Reg 3 2 1 0 → MAR 3 2 1 0 +1 → AC

To Reg 3 2 1 1

IAR 8 0 0 2 → MAR 8 0 0 2 +2 → IAR 8 0 0 4

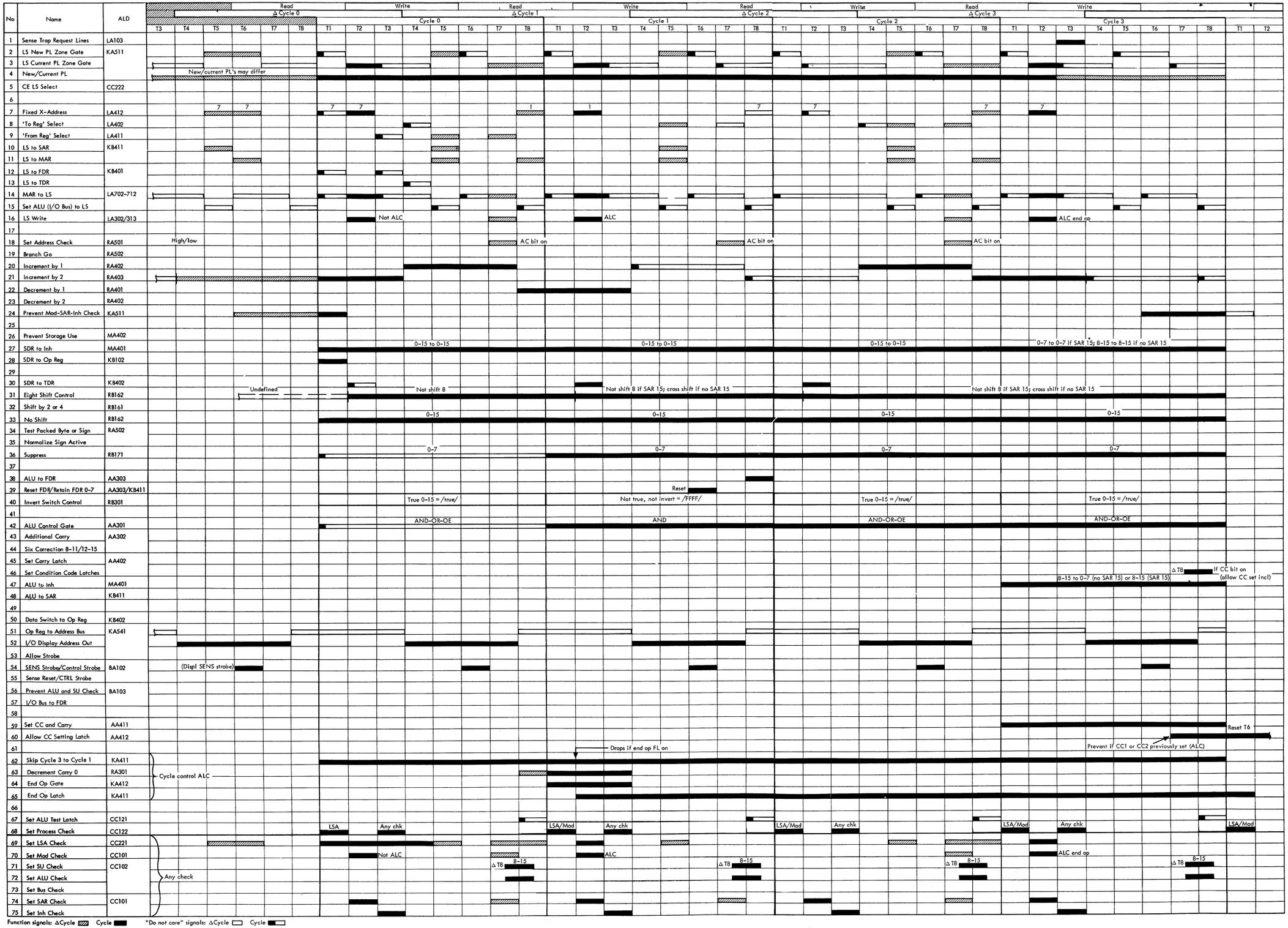
ALC end op: Yes / No — No action

SAR 3 2 1 0 — SAR 15

Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

Diagram 5-49. AND-OR-Exclusive OR-Byte or Halfword (XX, ALC) (Part 1 of 2) (03754A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59	Set CC and Carry	AA411
60	Allow CC Setting Latch	AA412
61		
62	Skip Cycle 3 to Cycle 1	KA411
63	Decrement Carry 0	RA301
64	End Op Gate	KA412
65	End Op Latch	KA411
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	

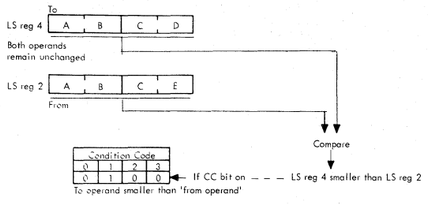


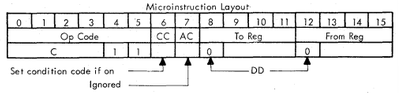
Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▭

● Diagram 5-49. AND-OR-Exclusive OR Byte or Halfword (XX, ALC) (Part 2 of 2) (03754A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

The 'from reg' is compared with the 'to reg'. 'To reg' and 'from reg' remain unchanged. The result of the comparison sets the condition code latches if the CC bit (instruction bit 6) is on. The comparison is done by subtracting the 'from operand' from the 'to operand'.

The address check is ignored.



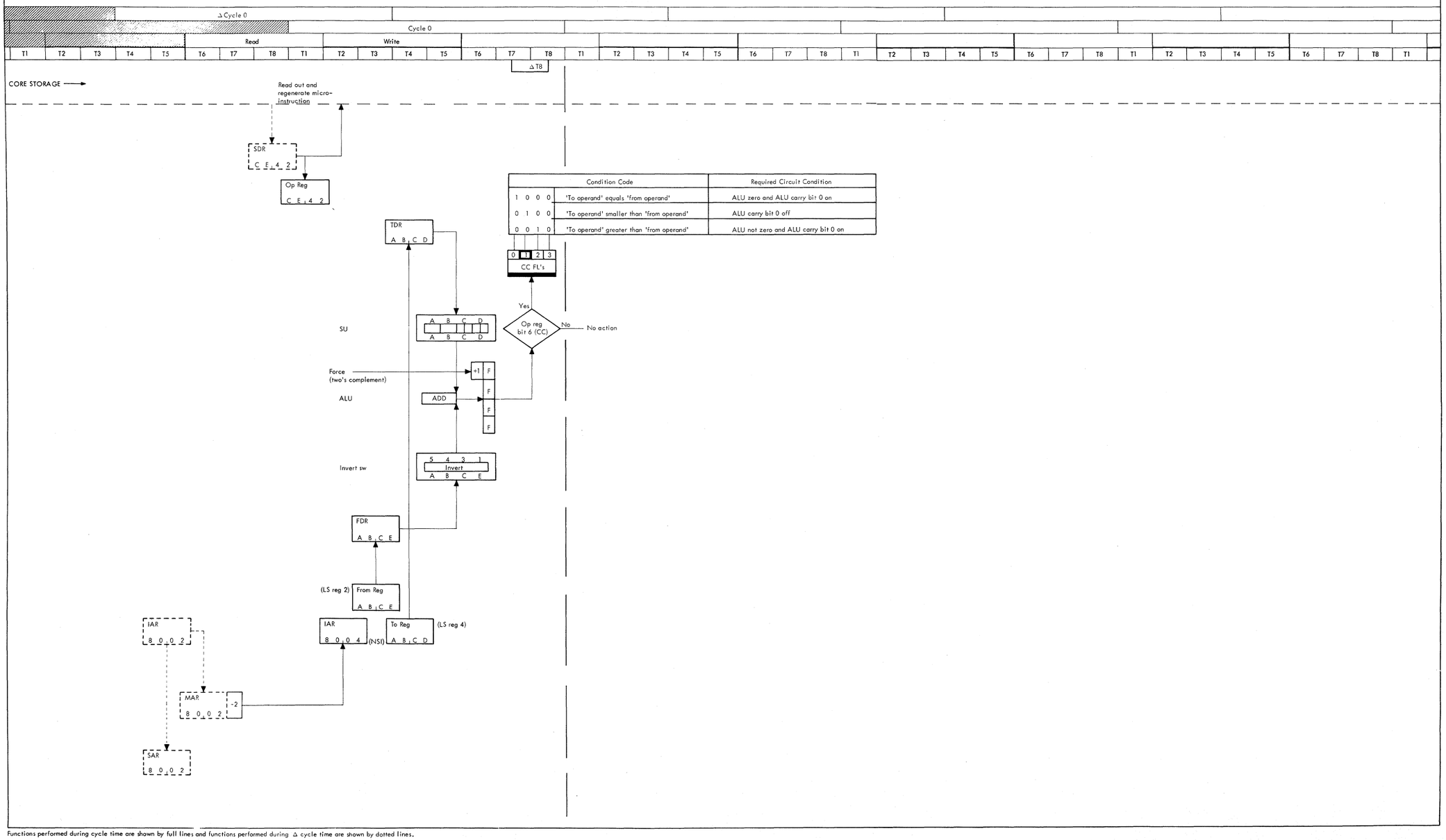


INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
CE42	CLC	4,2,CC	CC,R4,COMP,R2

Mnemonic
CLC
Format
FF
Type
DD

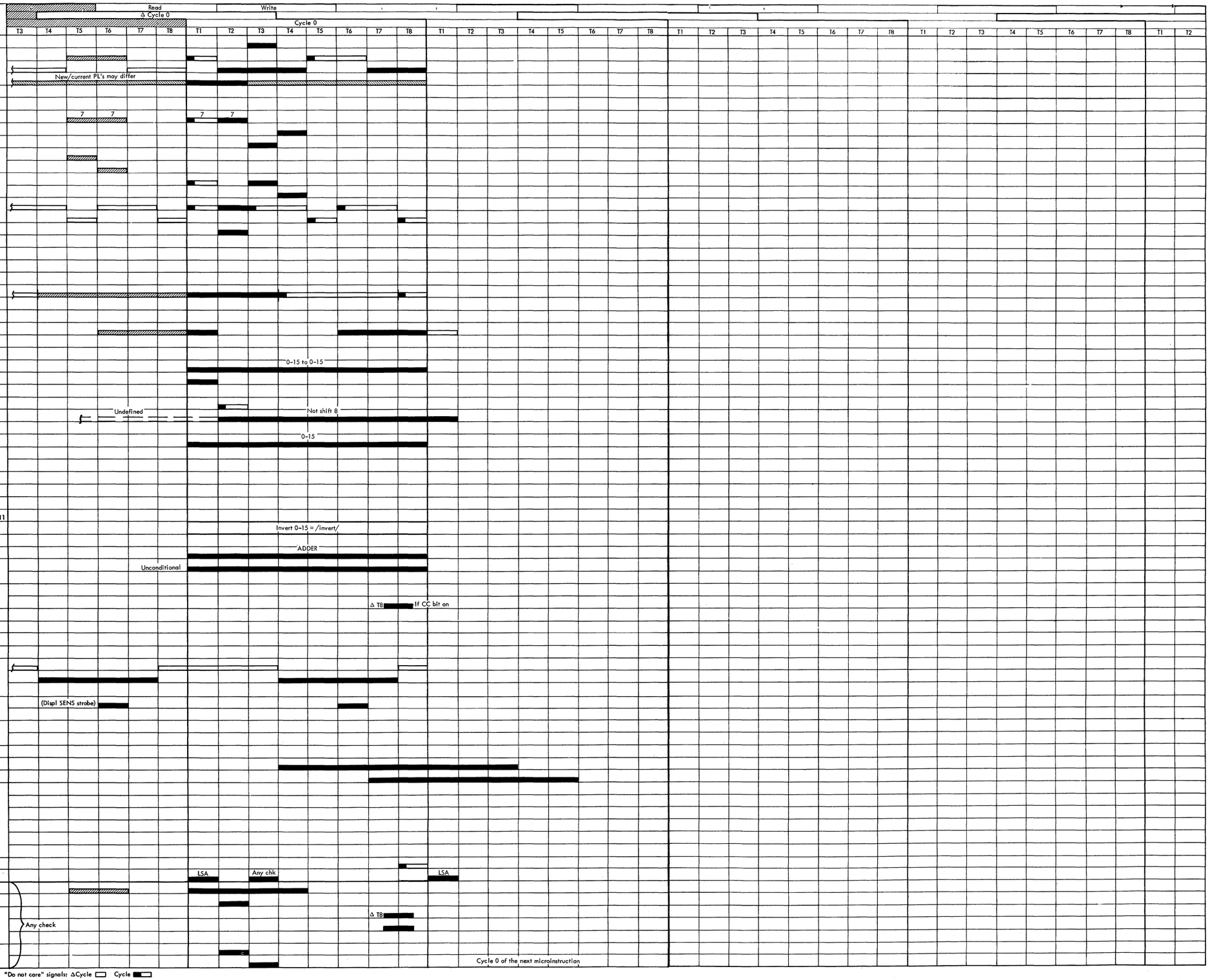
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
- ΔCycle
- Cycle



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59	Set CC and Carry	AA411
60	Allow CC Setting Latch	AA412
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▭

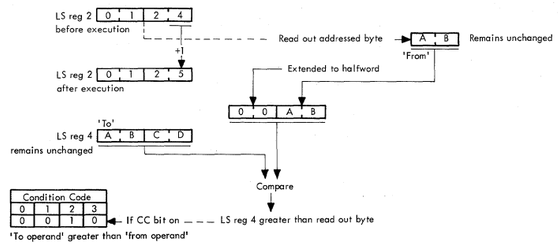
Diagram 5-50. Compare Logical Byte or Halfword (DD) (Part 2 of 2) (03755A)

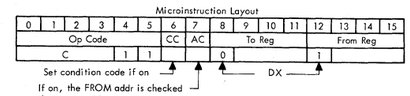
The byte addressed by the 'from reg' is compared with the halfword in the 'to reg'. The 'from' byte and the 'to reg' remain unchanged. The result of the comparison sets the condition code latches if the CC bit (instruction bit 6) is on.

The comparison is done by subtracting the 'from operand' from the 'to operand'. The 'from' byte is extended to a halfword by high-order zeros.

The 'from reg' address is incremented by 1.

If the AC bit (instruction bit 7) is on, an address check occurs when the 'from reg' address is outside customer area.





Mnemonic
CLC
Format
FF
Type
DX

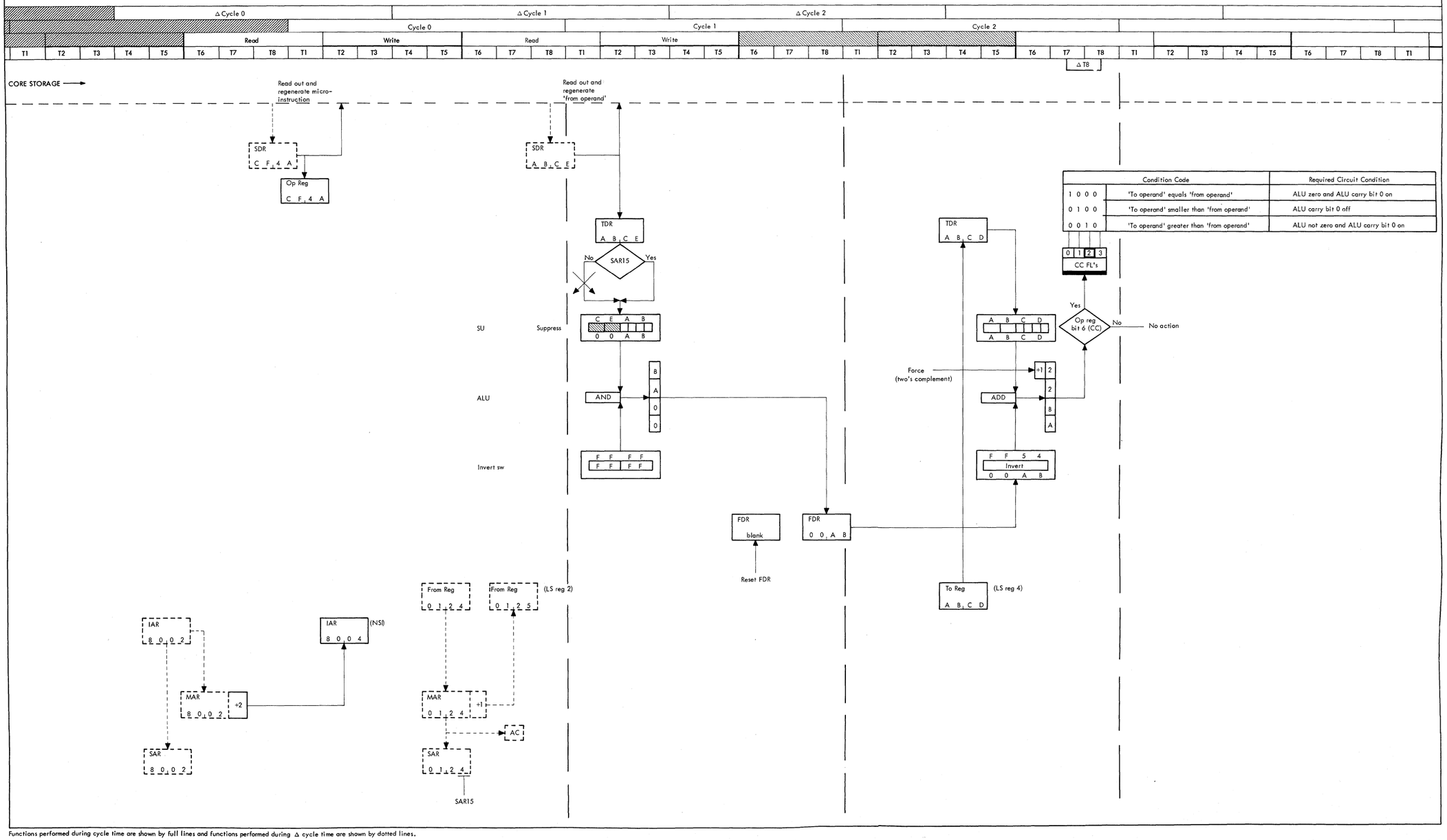
INST CF4A

MNEM OPERANDS CLC 4,2I,CC,AC

STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
CC,R4,COMP,'00'/BY(R2,AC,+1)

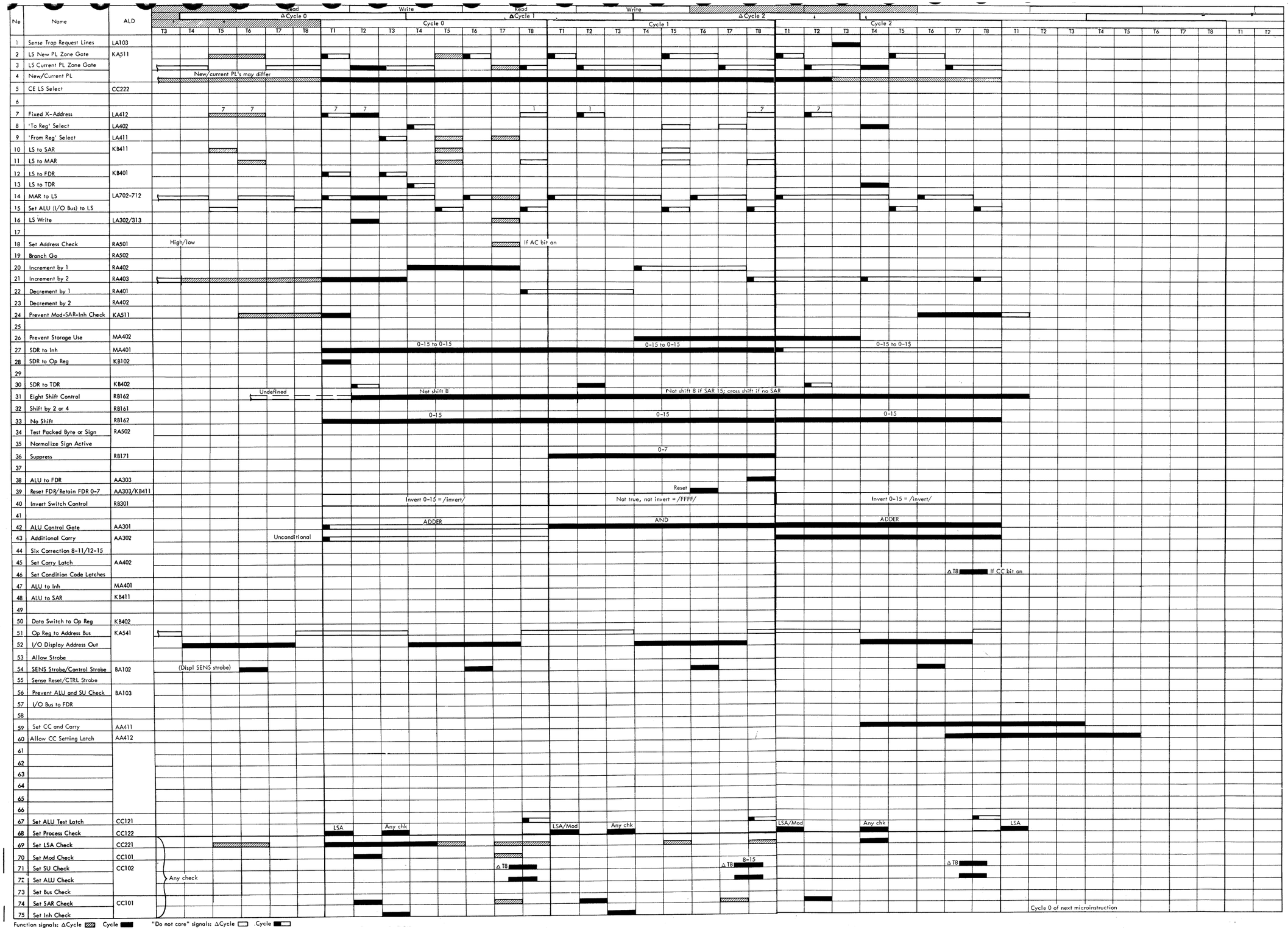
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59	Set CC and Carry	AA411
60	Allow CC Setting Latch	AA412
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▭

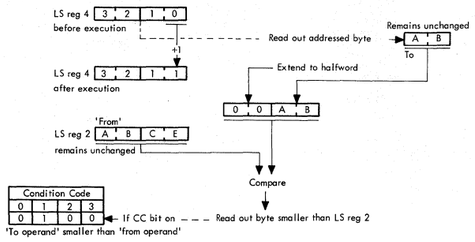
The halfword in the 'from reg' is compared with the byte addressed by the 'to reg'. The 'from reg' and the 'to'byte remain unchanged.

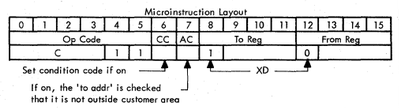
The result of the comparison sets the condition code latches if the CC bit (instruction bit 6) is on.

The comparison is done by subtracting the 'from operand' from the 'to operand'. The 'to' byte is extended to a halfword by high-order zeros.

The 'to reg' address is incremented by 1.

If the AC bit (instruction bit 7) is on, an address check occurs when the 'to reg' address is outside customer area.

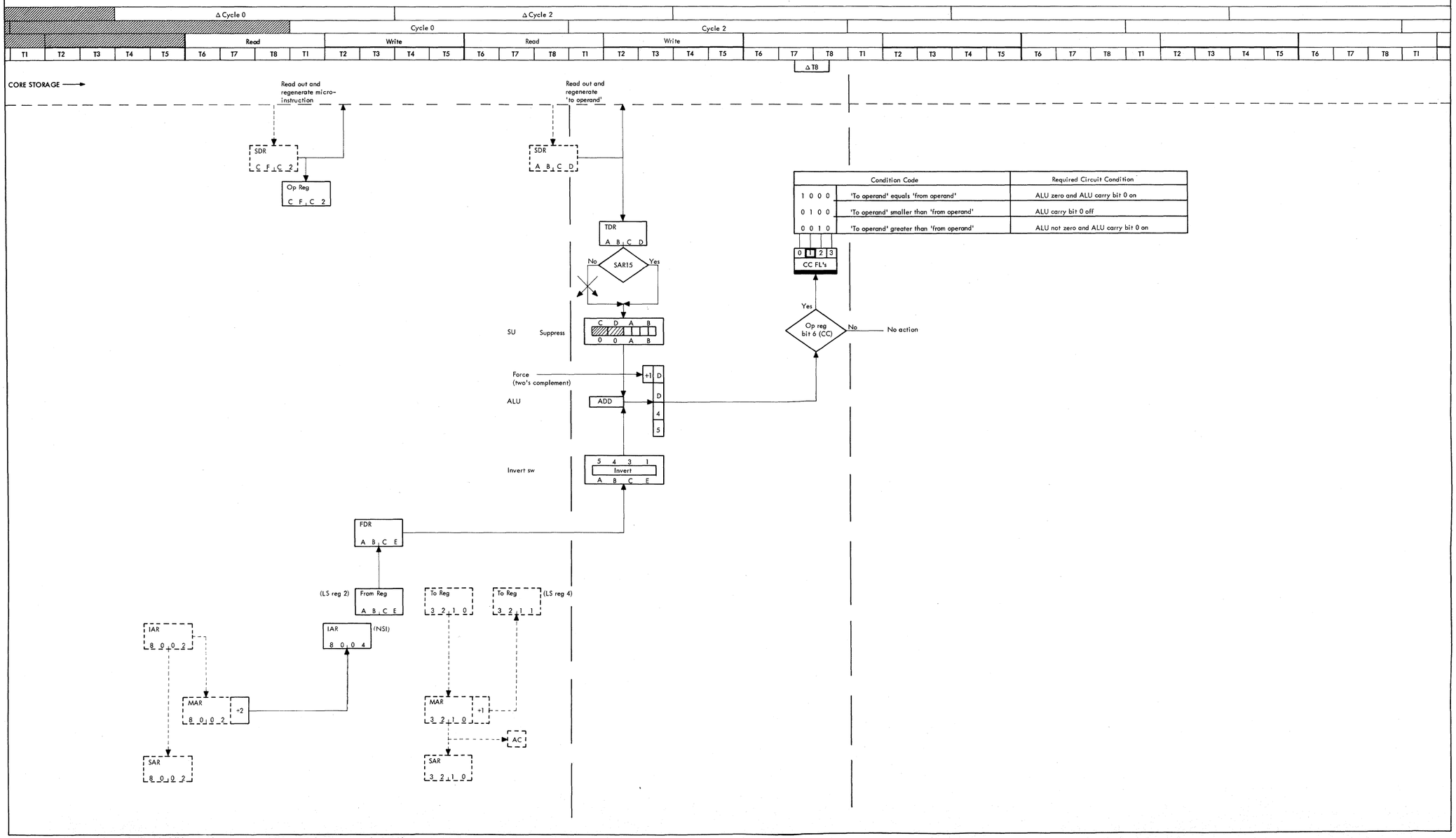




Mnemonic
CLC
Format
FF
Type
XD

INST MNEM OPERANDS STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX

CFC2 CLC 4I,2,CC,AC CC,'00'/BY(R4,AC,+1),COMP, R2

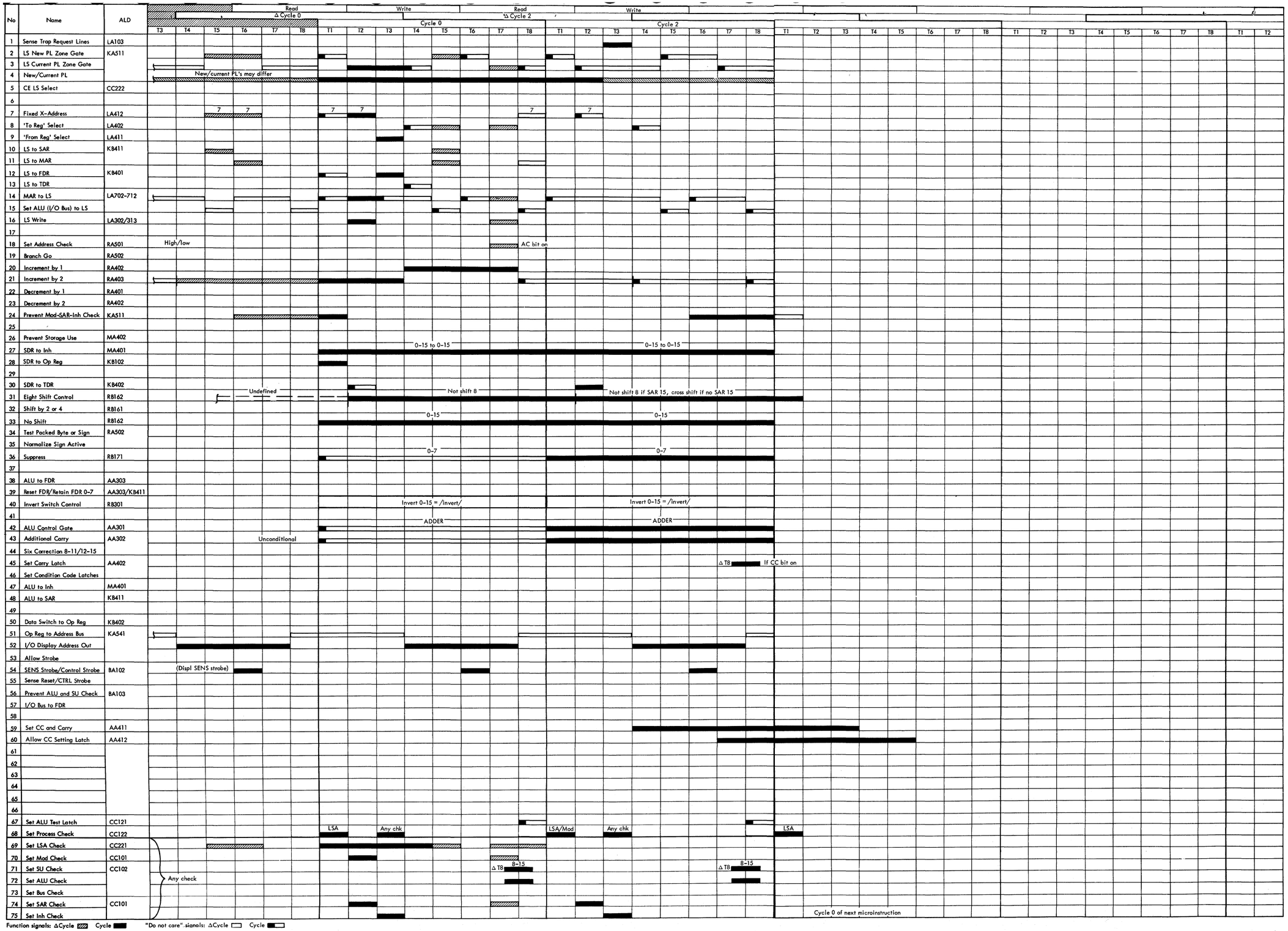


Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle

Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59	Set CC and Carry	AA411
60	Allow CC Setting Latch	AA412
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▭

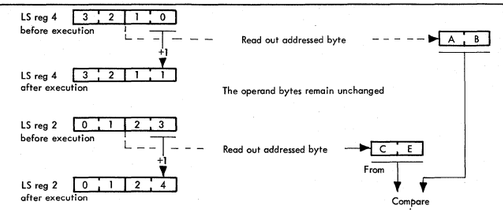
● Diagram 5-52. Compare Logical Byte or Halfword (XD) (Part 2 of 2) (03757A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

The byte addressed by the 'from reg' is compared with the byte addressed by the 'to reg'. Both bytes remain unchanged. The compare result sets the condition code latches if the CC bit (instruction bit 6) is on. The compare is done by subtracting the 'from operand' from the 'to operand'.

The 'from reg' and 'to reg' addresses are incremented by 1. If the AC bit (instruction bit 7) is on, an address check occurs when the 'from' or 'to' address is outside customer area.

The operation is performed in ALC mode when 'to reg' = 3 and 'from reg' = 5. LS register 1 contains the field length. The field length is the real number of bytes to be compared reduced by 1. The operand addresses are incremented by 1 every time a byte has been compared.

The ALC operation ends when either the field length is decremented below zero or the compare result becomes unequal.



Microinstruction Layout

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Op Code						CC	AC	To Reg				From Reg			
C				1	1			1				1			

Set condition code if on

If so, the 'from' and 'to' addr's are checked that they are not outside customer area

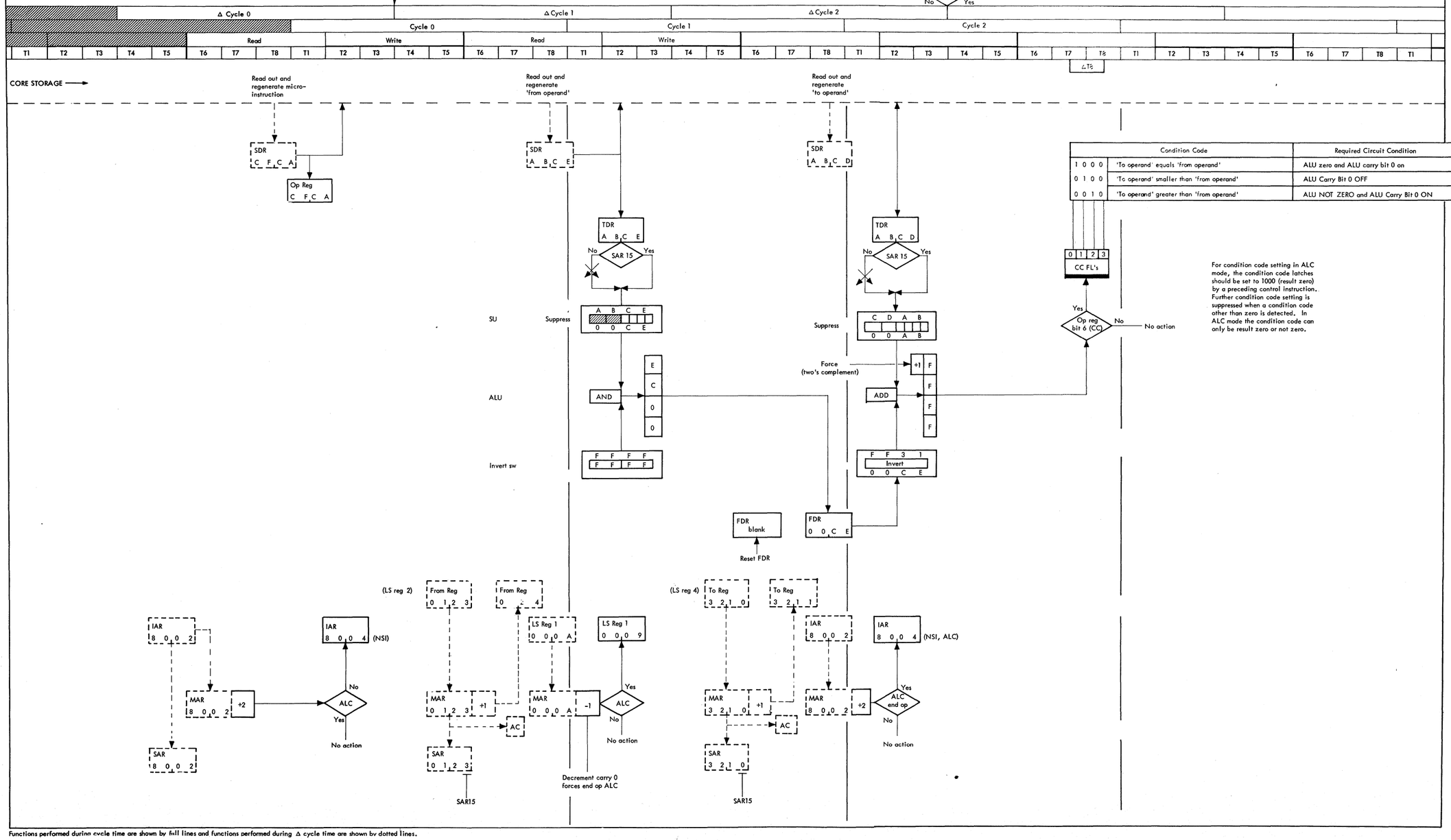
XX

Mnemonic
CLC
Format
FF
Type
XX (ALC)

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
CFCA	CLC	4I,2I,CC,AC	CC,BY(R4,AC,+1),COMP,BY(R2,AC,+1)
CFBD	CLC	3I,5I,CC,AC	CC,BY(R3,AC,+1),COMP,BY(R5,AC,+1), UNTIL R1,LT,0,OR BY 1,NE,BYZ

Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle



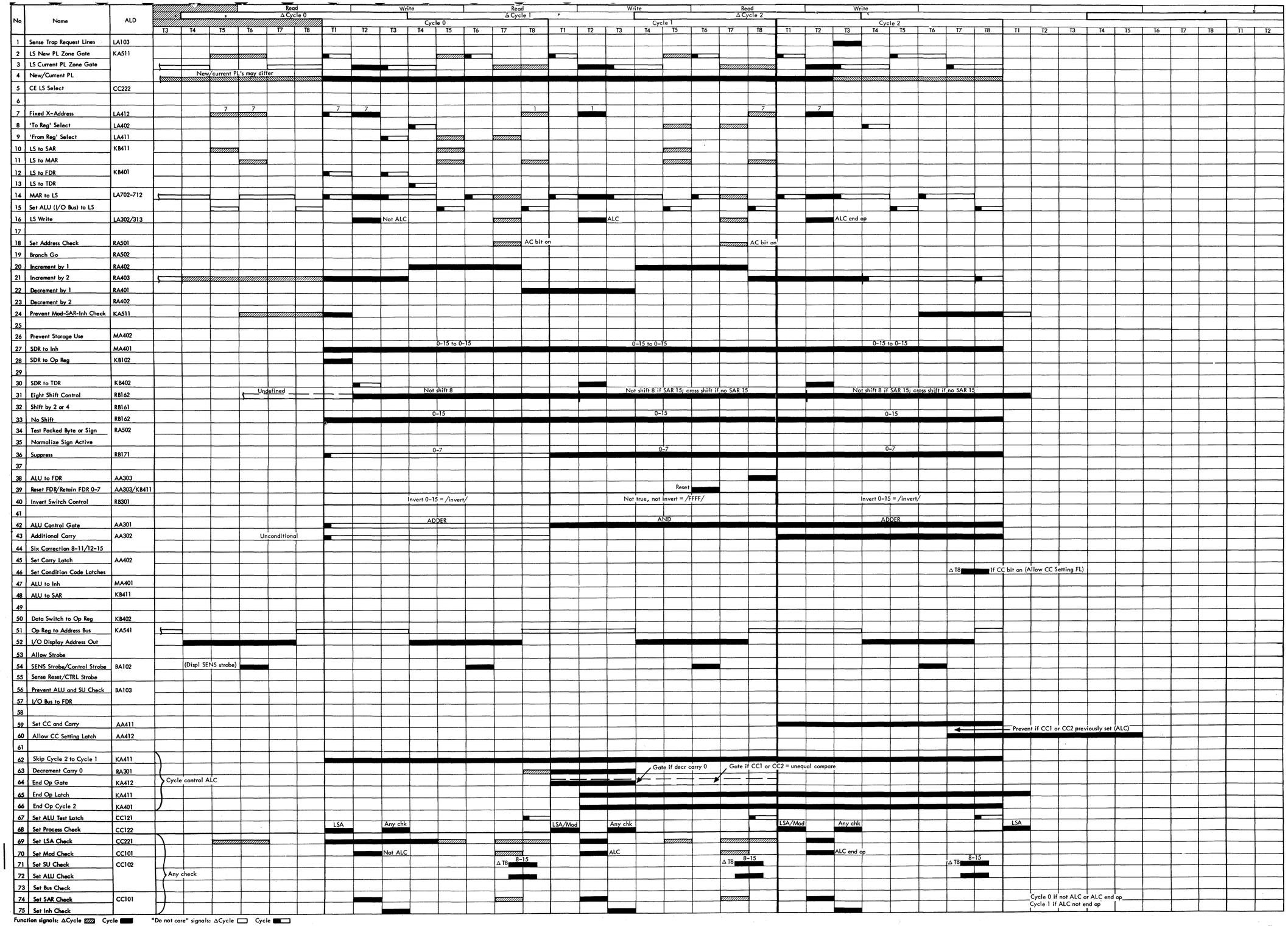
Condition Code		Required Circuit Condition
1 0 0 0	'To operand' equals 'from operand'	ALU zero and ALU carry bit 0 on
0 1 0 0	'To operand' smaller than 'from operand'	ALU Carry Bit 0 OFF
0 0 1 0	'To operand' greater than 'from operand'	ALU NOT ZERO and ALU Carry Bit 0 ON

For condition code setting in ALC mode, the condition code latches should be set to 1000 (result zero) by a preceding control instruction. Further condition code setting is suppressed when a condition code other than zero is detected. In ALC mode the condition code can only be result zero or not zero.

Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

Diagram 5-53. Compare Logical Byte or Halfword (XX, ALC) (Part 1 of 2) (03758A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59	Set CC and Carry	AA411
60	Allow CC Setting Latch	AA412
61		
62	Skip Cycle 2 to Cycle 1	KA411
63	Decrement Carry 0	RA301
64	End Op Gate	KA412
65	End Op Latch	KA411
66	End Op Cycle 2	KA401
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



● Diagram 5-53. Compare Logical Byte or Halfword (XX, ALC) (Part 2 of 2) (03758A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

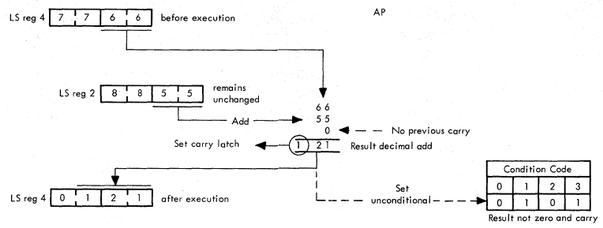
The two decimal digits in the low-order byte of the 'from reg' are added to the two decimal digits in the low-order byte of the 'to reg' (AP) or to zero (ZAP).

The result, which may consist of three decimal digits, is set into 'to reg'. The 'from reg' remains unchanged.

A previous carry (aux carry latch on) is implemented in the addition. A carry, out of the low-order byte, turns on the carry latch. The condition code latches are set.

A data check occurs when the low-order byte of the 'to reg' is not in packed decimal format.

Address check is ignored.



Microinstruction Layout

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
Op Code							AC	To Reg				From Reg				
D			0	0	0		0					0				AP
D			0	1	0		0					0				ZAP

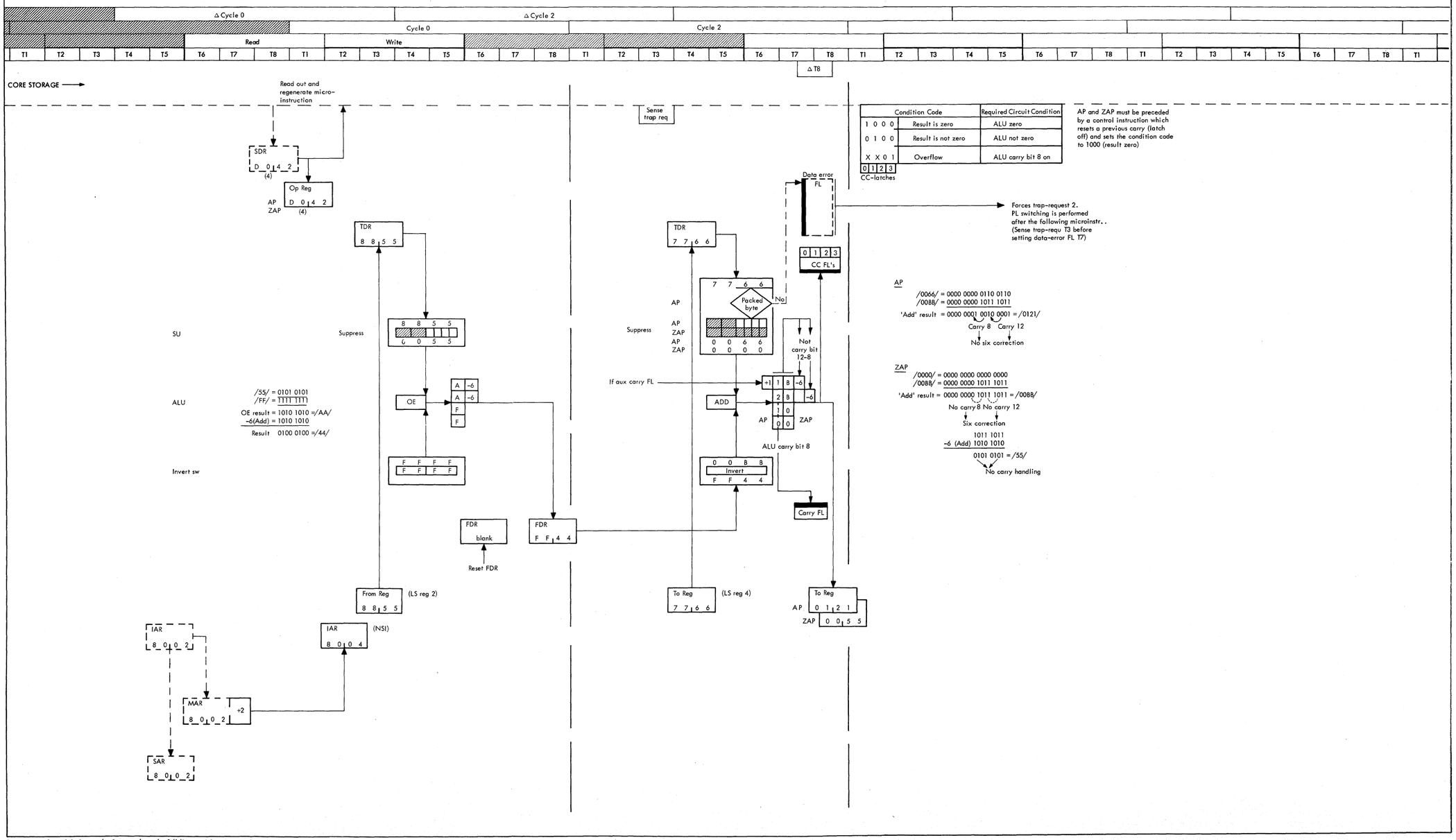
Ignored — DD

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
D042	AP	4,2	CC,C/R4+='00'/R4.8-15,D8,'00'/R2.8-15,D+,C
D442	ZAP	4,2	CC,C/R4+='00'/R2.8-15,D+,C

Mnemonic
AP
ZAP
Format
FF
Type
DD

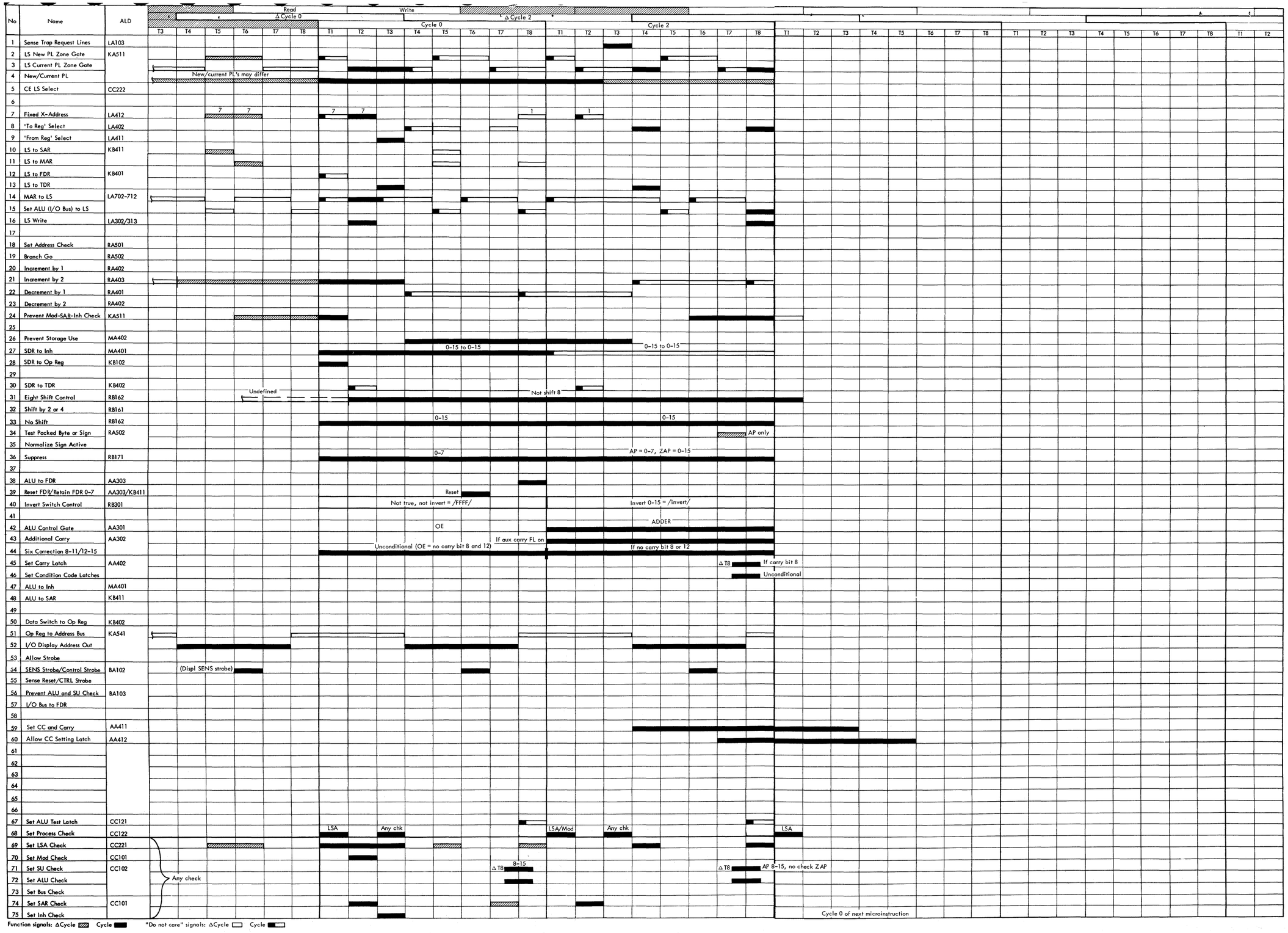
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59	Set CC and Carry	AA411
60	Allow CC Setting Latch	AA412
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▬

● Diagram 5-54. Add/Zero and Add Packed Byte (DD) (Part 2 of 2) (03759A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

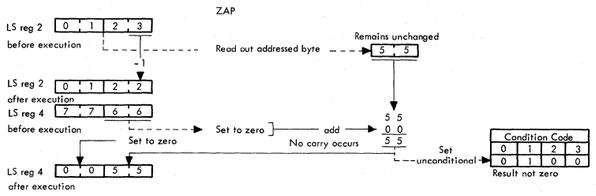
The two decimal digits in the byte addressed by the 'from reg' are added to the two decimal digits in the low-order byte of the 'to reg' (AP) or to zero (ZAP). The result, which may consist of three decimal digits, is set into 'to reg'. The 'from' byte remains unchanged.

A previous carry (aux carry latch on) is implemented in the addition. A carry, out of the low-order byte, turns on the carry latch. The condition code latches are set.

A data check occurs when the low-order byte of the 'to reg' is not in packed format.

The 'from reg' address is decremented by 1. If the AC bit (instruction bit 7) is on, an address check occurs when the 'from reg' address is outside customer area.

ZAP



Microinstruction Layout

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
Op Code							AC	To Reg				From Reg				
D				0	0	0		0				1				AP
D				0	1	0		0				1				ZAP

If on, the 'from addr' is checked that it is not outside customer area

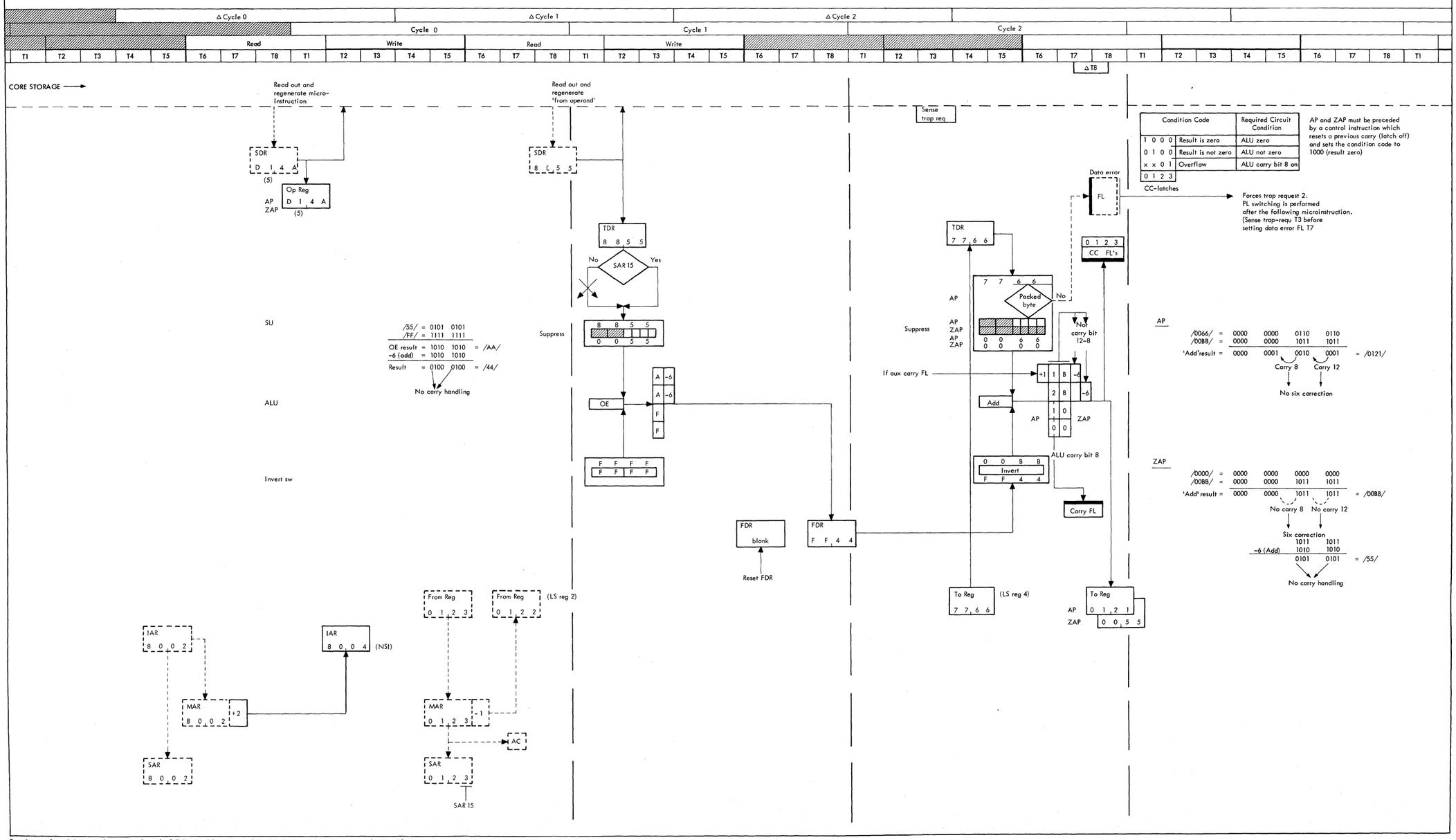
DX

Mnemonic
AP
ZAP
Format
FF
Type
DX

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
D14A	AP	4,2I,AC	CC,C/R4+='00'/R4.8-15,D+,'00'/BY(R2,AC,-1),D+,C
D54A	ZAP	4,2I,AC	CC,C/R4+='00'/BY(R2,AC,-1),D+,C

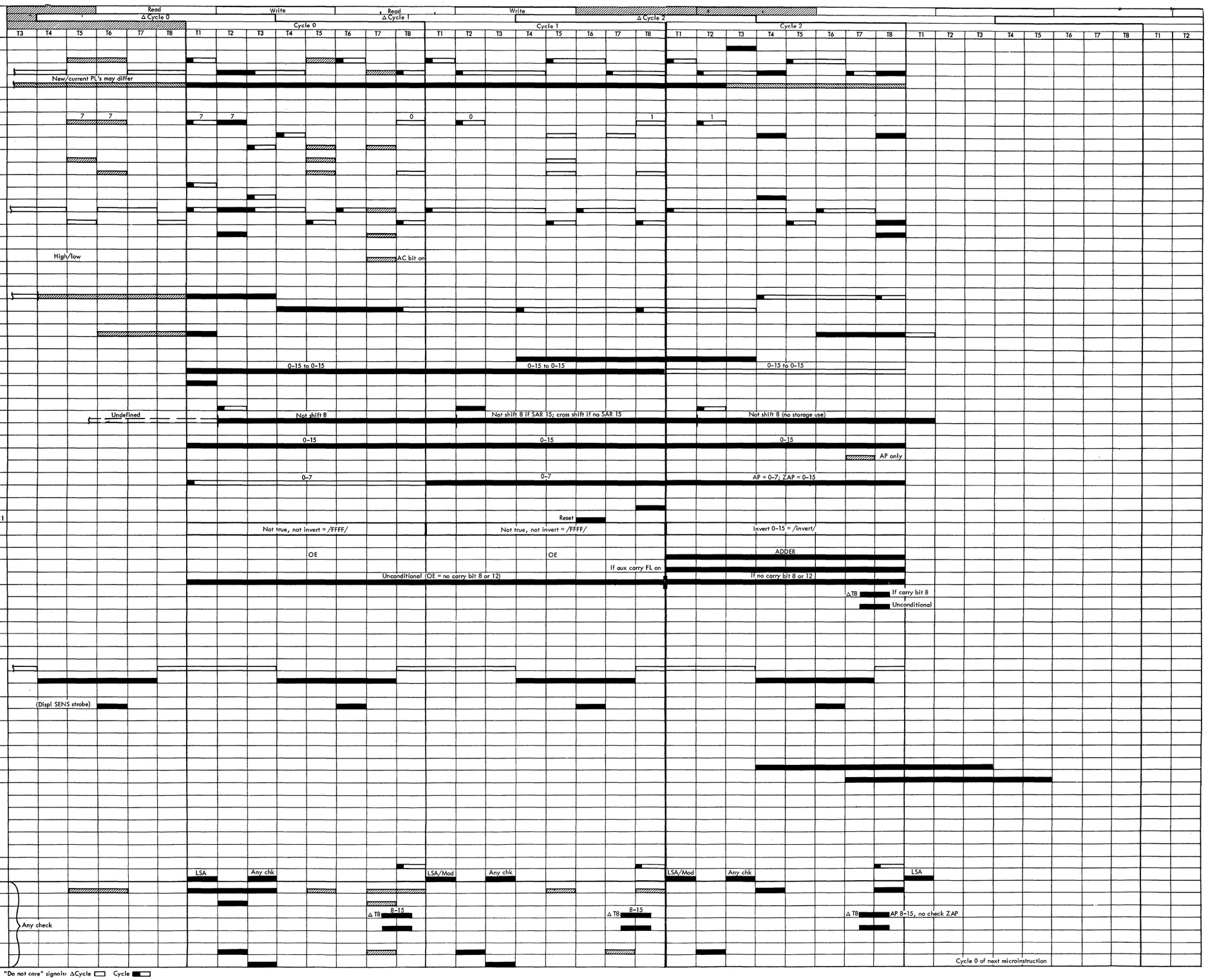
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59	Set CC and Carry	AA411
60	Allow CC Setting Latch	AA412
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▬

● Diagram 5-55. Add/Zero and Add Packed Byte (DX) (Part 2 of 2) (03760A)

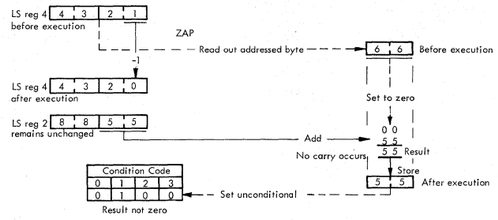
The two decimal digits in the low-order byte of the 'from reg' are added to the two decimal digits in the byte addressed by the 'to reg' (AP) or to zero (ZAP). The result (low-order two decimal digits) is set into the byte addressed by the 'to reg'. The 'from reg' remains unchanged.

A previous carry (aux carry latch on) is implemented in the addition. A carry out of the low-order byte turns on the carry latch. The condition code latches are set.

A data check occurs when the low-order byte of the 'from reg' or the byte addressed by the 'to reg' is not in packed decimal format.

The 'to reg' address is decremented by 1.

If the AC bit (instruction bit 7) is on, an address check occurs when the 'to reg' address is outside customer area.



Microinstruction Layout

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
Op Code							AC	To Reg				From Reg				
D				0	0	0		1				0				AP
D				0	1	0		1				0				ZAP

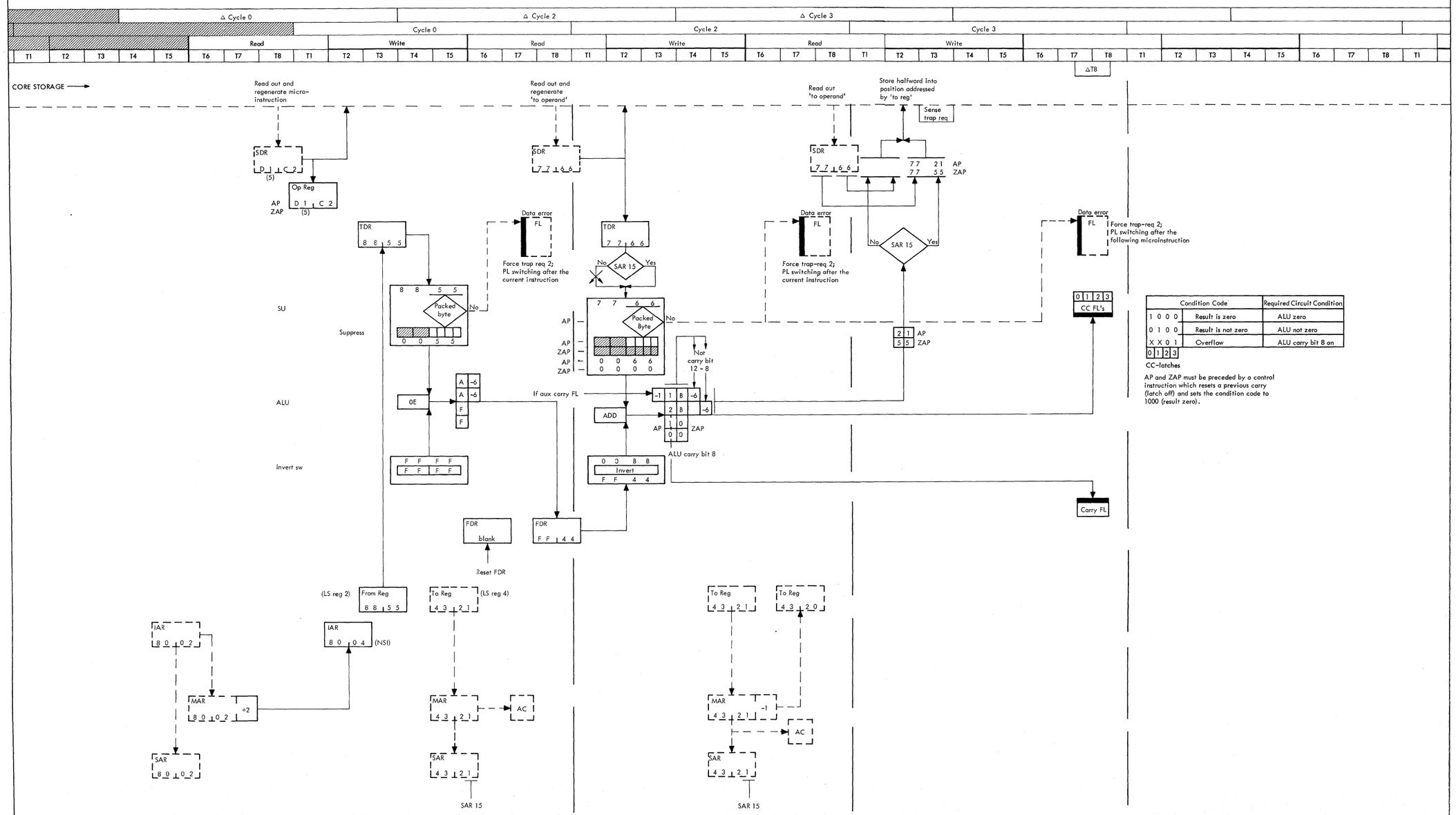
If on, the 'to addr' is checked that it is not outside customer area — XD

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
D1C2	AP	4I,2,AC	CC,C/BY(R4,AC)+=BY(R4,-1),D+,R2.8-15,D+,C
D5C2	ZAP	4I,2,AC	CC,C/BY(R4,AC,-1)+=R2.8-15,D+,C

Mnemonic
AP
ZAP
Format
FF
Type
XD

Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle



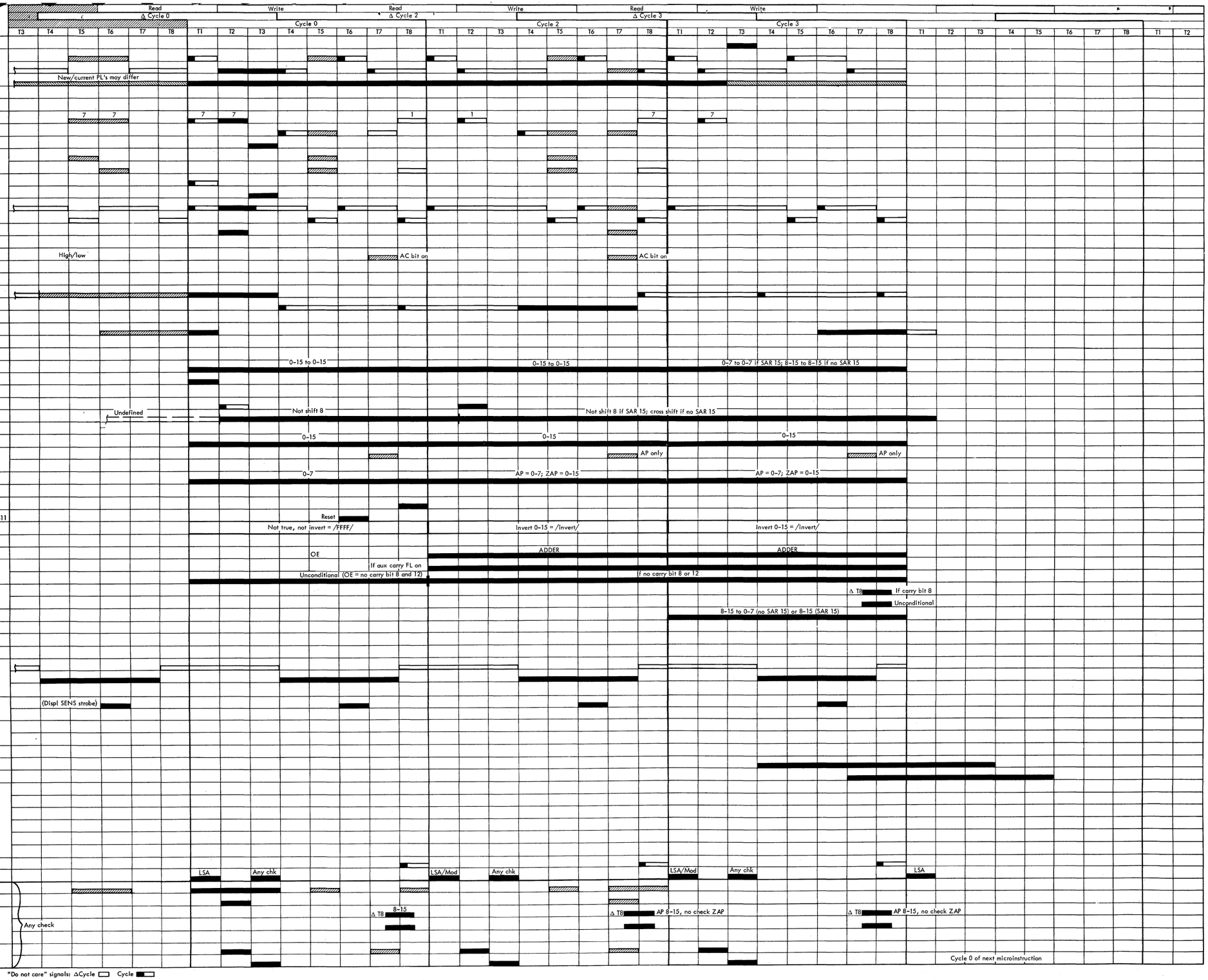
Condition Code		Required Circuit Condition
1 0 0 0	Result is zero	ALU zero
0 1 0 0	Result is not zero	ALU not zero
X X 0 1	Overflow	ALU carry bit 8 on

0 1 2 3
CC-latches

AP and ZAP must be preceded by a control instruction which resets a previous carry (latch off) and sets the condition code to 1000 (result zero).

Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59	Set CC and Carry	AA411
60	Allow CC Setting Latch	AA412
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



Function signals: ΔCycle Cycle "Do not care" signals: ΔCycle Cycle

● Diagram 5-56. Add/Zero and Add Packed Byte (XD) (Part 2 of 2) (03761A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

The two decimal digits in the byte addressed by the 'from reg' are added to the two decimal digits in the byte addressed by the 'to reg' (AP) or to zero (ZAP). The result (two decimal digits) is set into the byte addressed by the 'to reg'. The 'from' byte remains unchanged.

A previous carry (aux carry latch on) is implemented in the addition. A carry, out of the low-order byte, turns on the carry latch. The condition code latches are set. A data check occurs when the 'from' byte or the 'to' byte is not in packed decimal format.

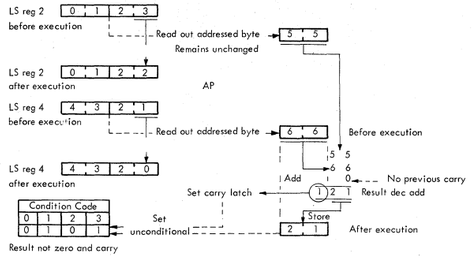
Both operand addresses are decremented by 1. If the AC bit (instruction bit 7) is on, an address check occurs when the operand addresses are outside customer area.

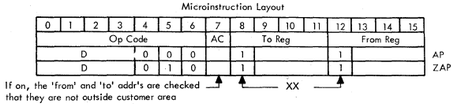
The operation is performed in ALC mode when 'to reg' = 3 and 'from reg' = 5. Each operand has its own field length and the field lengths may be different. LS register 0 contains the field length of the 'from operand'. LS register 1 contains the field length of the 'to operand'.

The field length is the real number of bytes in an operand field reduced by 1.

The operand addresses are incremented by 1 every time a byte is operated.

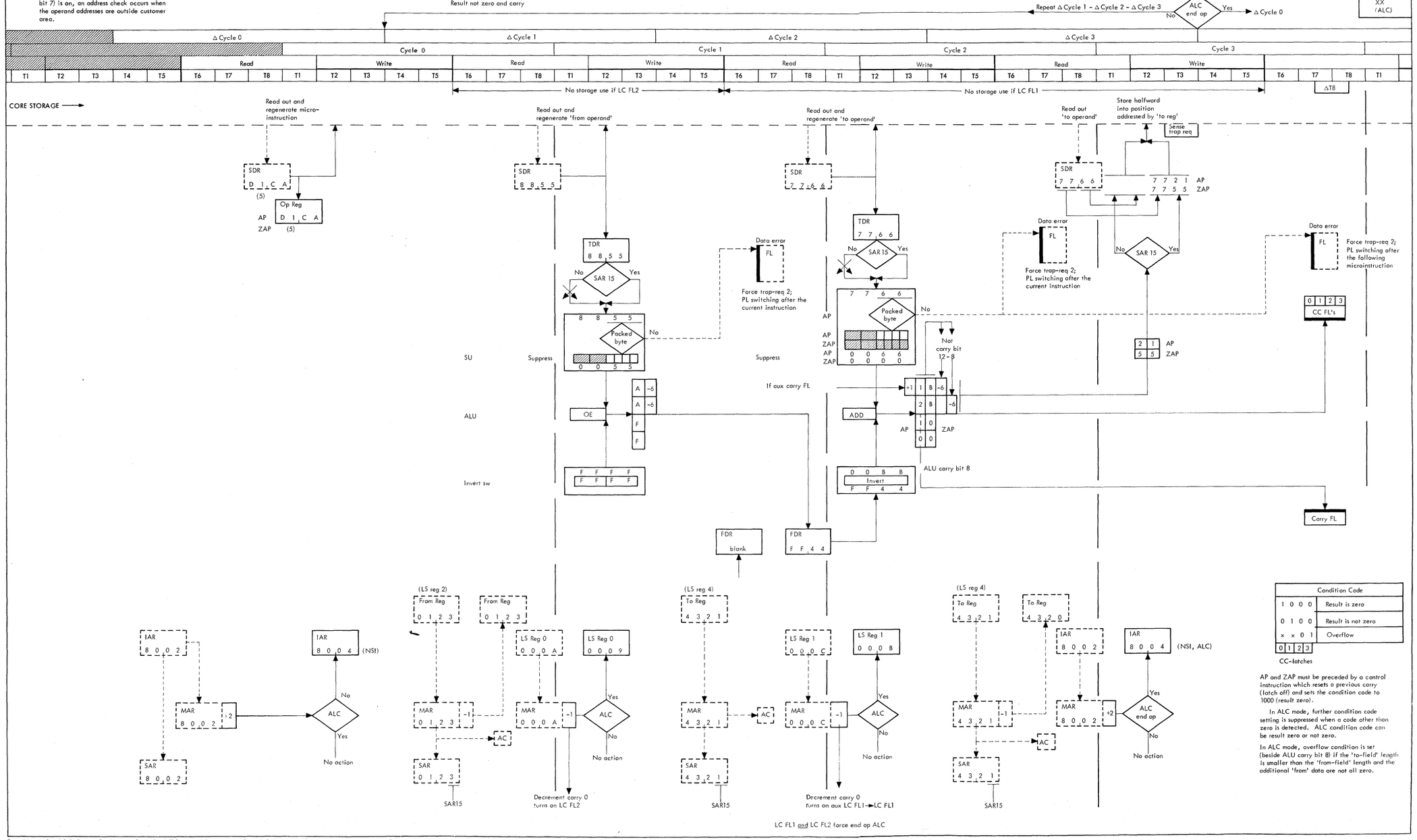
If the 'to operand' field is too small to accept all digits of the 'from operand' field the condition code is set to overflow (CC latch 3 on).





INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
D1CA	AP	4I,2I,AC	CC,C/BY(R4,AC)+=BY(R4,-1),D+,BY(R2,AC,-1),D+,C
D5CA	ZAP	4I,2I,AC	CC,C/BY(R4,AC,-1)+=BY(R2,AC,-1),D+,C
D1BD	AP	3I,5I,AC	CC,C/BY(R3,AC,UNTIL R1,LT,0)+=BY(R3,-1),D+,BY(R5,AC,-1,UNTIL R0, LT,0),D+,C

Mnemonic
AP
ZAP
Format
FF
Type
XX (ALC)



Condition Code	
1 0 0 0	Result is zero
0 1 0 0	Result is not zero
× × 0 1	Overflow
0 1 2 3	

CC-latches

AP and ZAP must be preceded by a control instruction which resets a previous carry (latch off) and sets the condition code to 1000 (result zero).

In ALC mode, further condition code setting is suppressed when a code other than zero is detected. ALC condition code can be result zero or not zero.

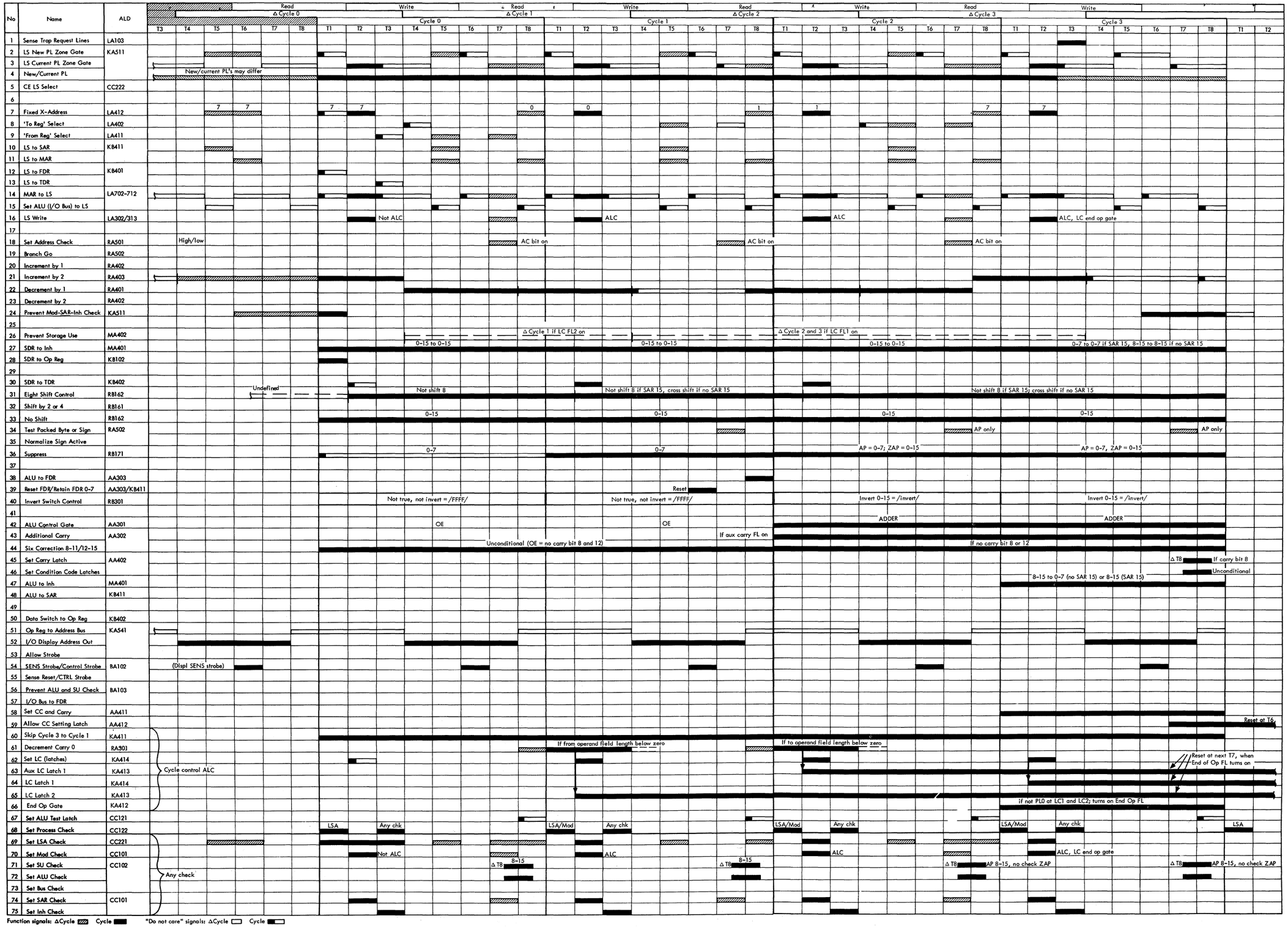
In ALC mode, overflow condition is set (beside ALU carry bit 8) if the 'to-field' length is smaller than the 'from-field' length and the additional 'from' data are not all zero.

Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle

Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58	Set CC and Carry	AA411
59	Allow CC Setting Latch	AA412
60	Skip Cycle 3 to Cycle 1	KA411
61	Decrement Carry 0	RA301
62	Set LC (latches)	KA414
63	Aux LC Latch 1	KA413
64	LC Latch 1	KA414
65	LC Latch 2	KA413
66	End Op Gate	KA412
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▭

● Diagram 5-57. Add/Zero and Add Packed Byte (XX, ALC) (Part 2 of 2) (03762A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

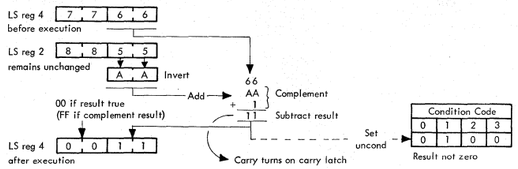
For SP, the two decimal digits in the low-order byte of the 'from reg' are subtracted from the two decimal digits in the low-order byte of the 'to reg'. The result is set into 'to reg'.

For PPC, the tens complement of the two decimal digits in the 'low-order' byte of the 'from reg' is set into 'to reg'. The 'from reg' remains unchanged.

A previous carry (aux carry latch on) is implemented in the operation.

Before initiating SP or PPC, the previous carry must be simulated by turning on the carry latch by a control /10/, bit 11 to obtain the correct complement.

A carry, out of the low-order byte, turns on the carry latch. The condition code latches are set. A data check occurs when the low-order byte of the 'to reg' is not in packed decimal format. Address check is ignored.



Microinstruction Layout

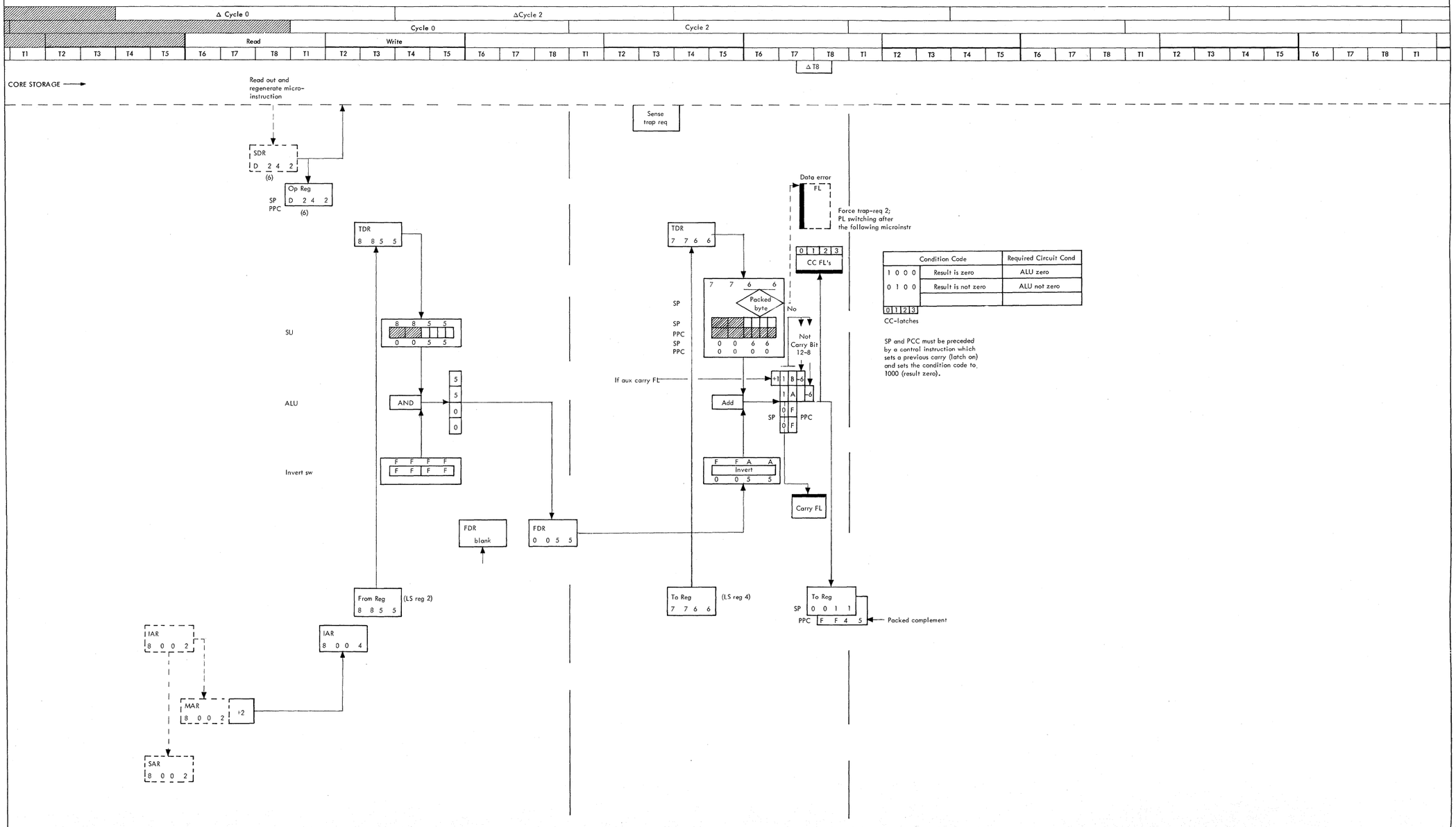
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
Op Code							AC	To Reg				From Reg				
D			0	0	1		0					0				SP
D			0	1	1		0					0				PPC
Ignored								DD								

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
D242	SP	4,2	CC,C/R4+= '00'/R4.8-15,D-,'00'/R2.8-15,D-,C
D642	PPC	4,2	CC,C/R4+= 'FF'/X,X = '99',D-,R2.8-15,D+,C

Mnemonic
SP
PPC
Format
FF
Type
DD

Note: For "Do not care" functions refer to timing chart below.

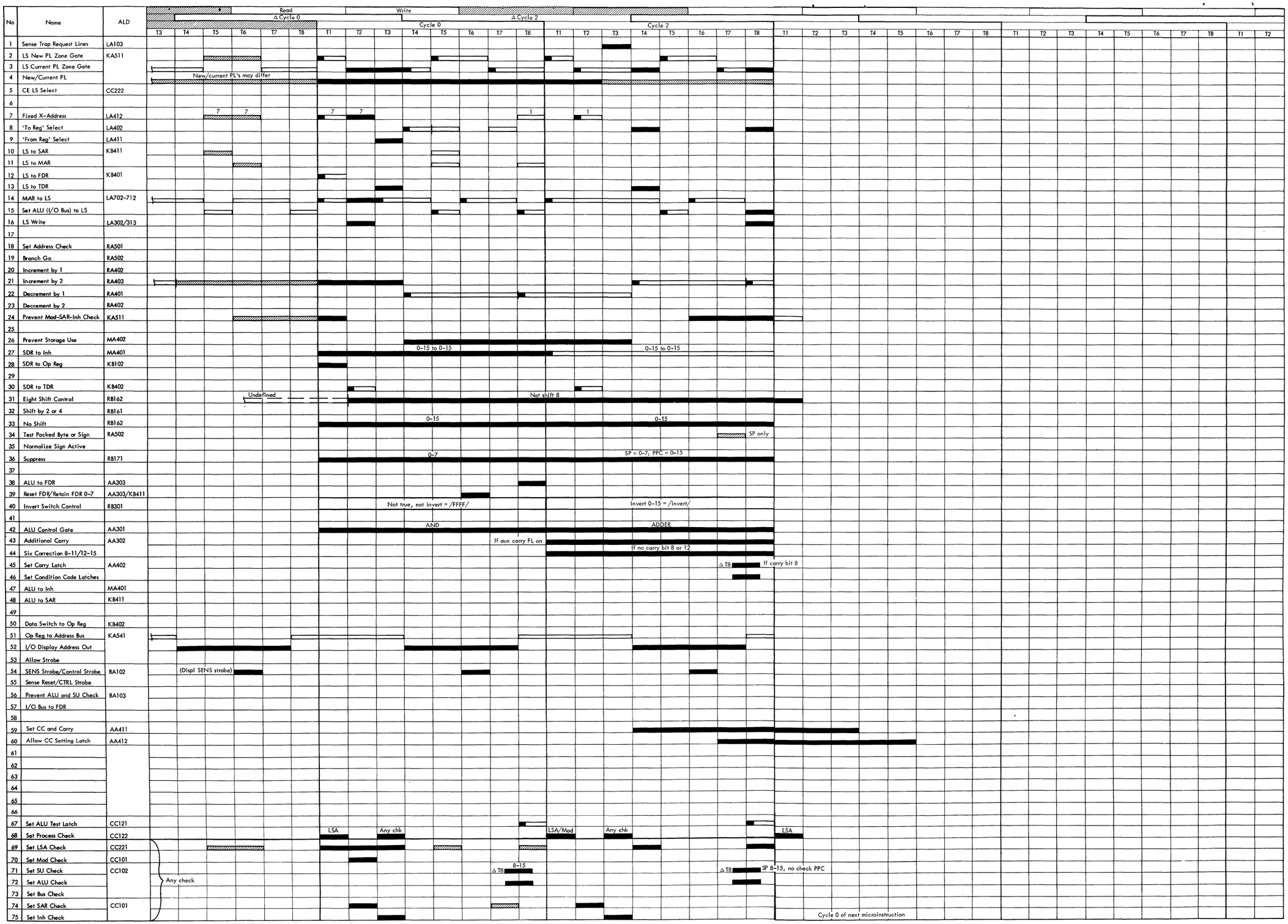
"Do not care" signals:
ΔCycle
Cycle



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

Diagram 5-58. Subtract Packed Byte/Perform Packed Complement (DD) (Part 1 of 2) (03763) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59	Set CC and Carry	AA411
60	Allow CC Setting Latch	AA412
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▭

● **Diagram 5-58. Subtract Packed Byte/Perform Packed Complement (DD) (Part 2 of 2)** (03763A)

For SP, the two decimal digits in the byte addressed by the 'from reg' are subtracted from the two decimal digits in the low-order byte of the 'to reg'. The result is set into 'to reg'. For PPC, the tens complement of the two decimal digits in the byte addressed by the 'from reg' is set into 'to reg'. The 'from' byte remains unchanged.

A previous carry (aux carry latch on) is implemented in the operation.

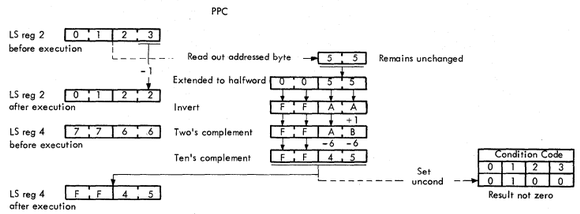
Before initiating SP or PPC, the previous carry must be simulated by turning on the carry latch by a control/10/, bit 11, to obtain the correct complement.

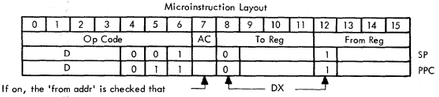
A carry, out of the low-order byte, turns on the carry latch. The condition code latches are set.

A data check occurs when the low-order byte of the 'to reg' is not in packed decimal format.

The 'from reg' address is decremented by 1.

If the AC bit (instruction bit 7) is on, an address check occurs when the 'from address' is outside customer area.



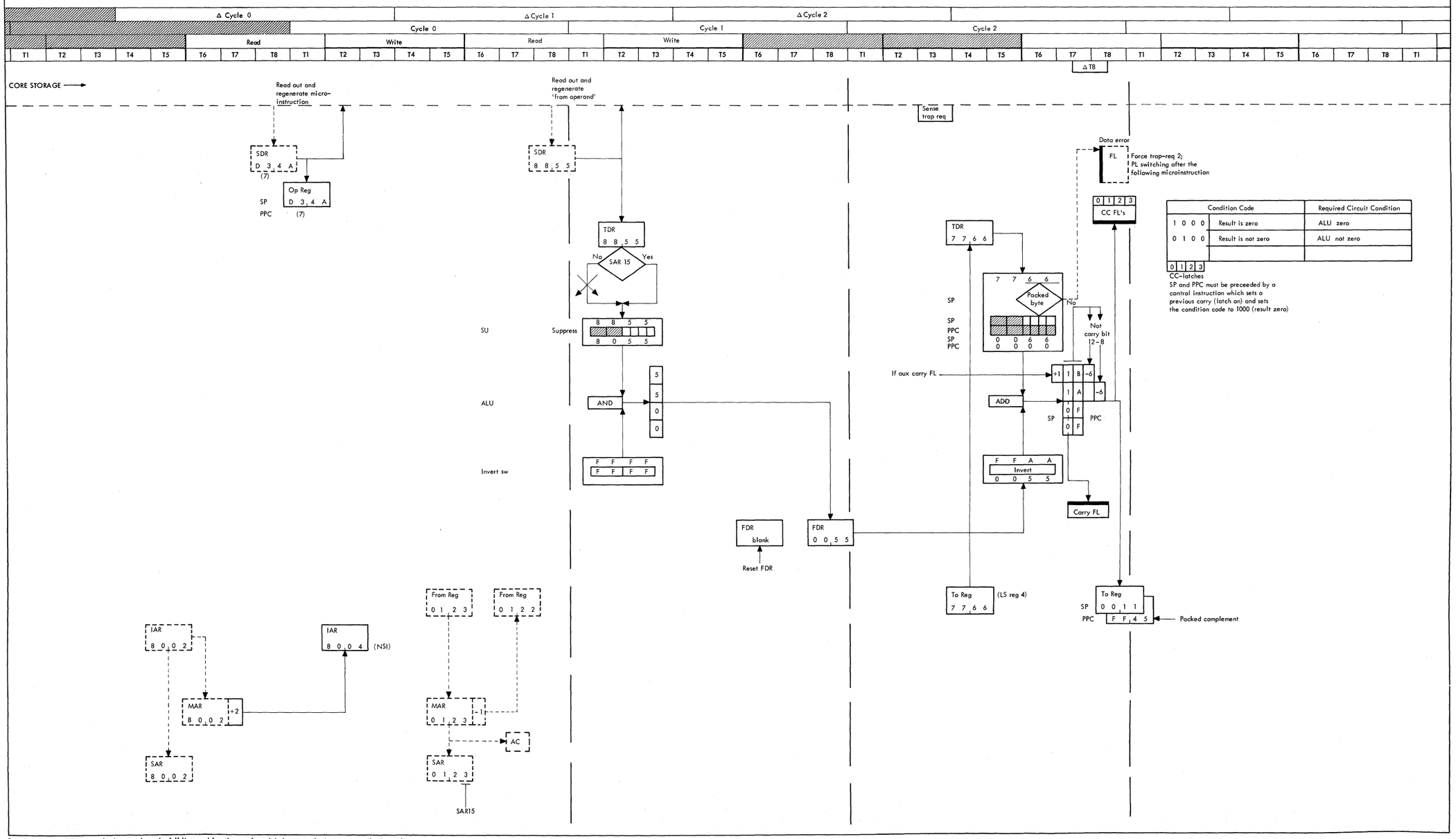


Mnemonic
SP
PPC
Format
FF
Type
DX

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
D34A	SP	4,2I,AC	CG,C/R4₩= '00$/R4.8-15,D-,'00$/BY(R2,AC,-1),D-,C
D74A	PPC	4,2I,AC	CG,C/R4₩=FF$/X ,X = '99$,D-,BY(R2,AC,-1),D+,C

Note: For "Do not care" functions refer to timing chart below.

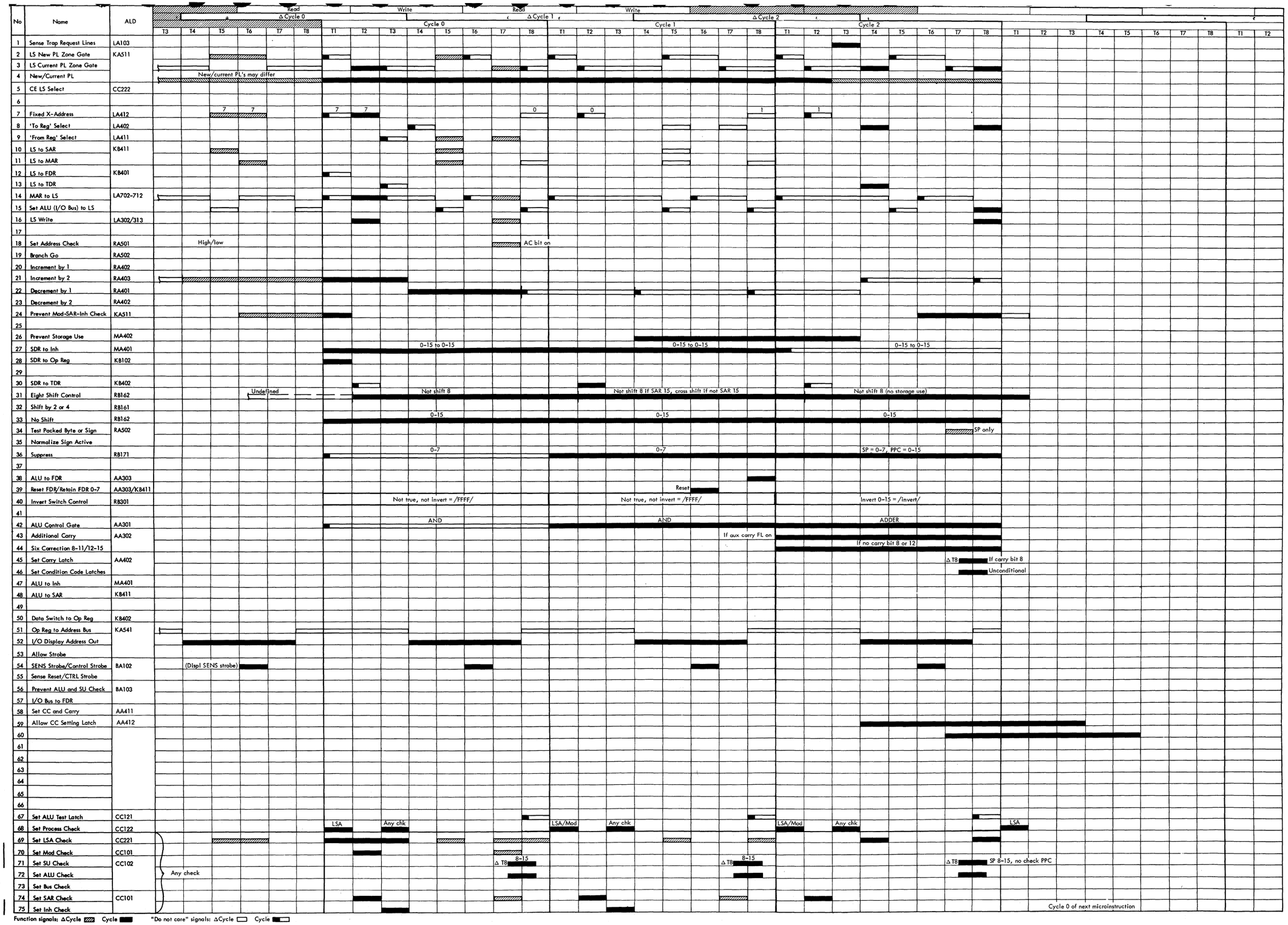
"Do not care" signals:
ΔCycle
Cycle



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

Diagram 5-59. Subtract Packed Byte/Perform Packed Complement (DX) (Part 1 of 2) (03764) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58	Set CC and Carry	AA411
59	Allow CC Setting Latch	AA412
60		
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▭

● **Diagram 5-59. Subtract Packed Byte/Perform Packed Complement (DX) (Part 2 of 2)** (03764A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

For SP, the two decimal digits in the low-order byte of the 'from reg' are subtracted from the two decimal digits in the byte addressed by the 'to reg'. The result is set into the byte addressed by the 'to reg'.

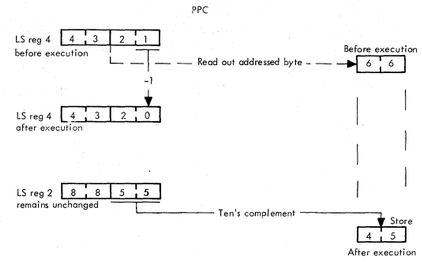
For PPC, the tens complement of the two decimal digits in the low-order byte of the 'from reg' is set into the byte addressed by the 'to reg'. The 'from reg' remains unchanged.

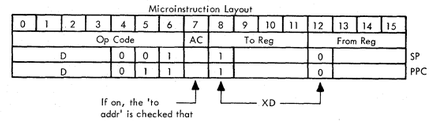
A previous carry (aux carry latch on) is implemented in the operation. Before initiating SP or PPC, the previous carry must be simulated by turning on the carry latch by a control/10/, bit 11, to obtain the correct complement. A carry out of the low-order byte turns on the carry latch. The condition code latches are set.

A data check occurs when the low-order byte in the 'from reg' or the byte addressed by the 'to reg' is not in packed decimal format.

The 'to reg' address is decremented by 1.

If the AC bit (instruction bit 7) is on, an address check occurs when the 'to address' is outside customer area.



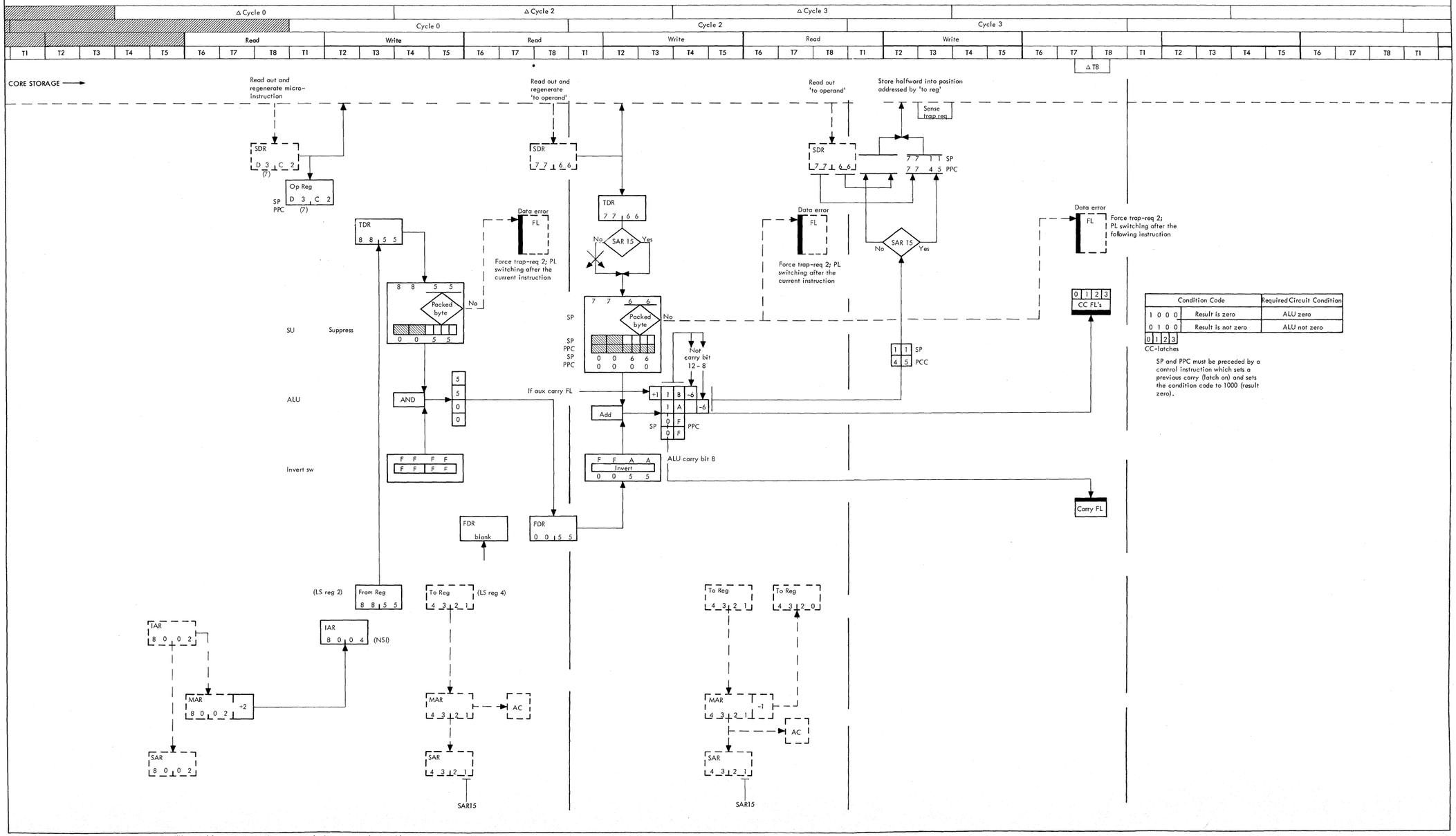


INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
D3C2	SP	4I,2,AC	CC,C/BY(R4,AC)+=BY(R4,-1),D-,R2.8-15,D-,C
D7C2	PPC	4I,2,AC	CC,C/BY(R4,AC,-1)-=#99',D-,R2.8-15,D+,C

Mnemonic
SP
PPC
Format
FF
Type
XD

Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle



Condition Code		Required Circuit Condition
1 0 0 0	Result is zero	ALU zero
0 1 0 0	Result is not zero	ALU not zero

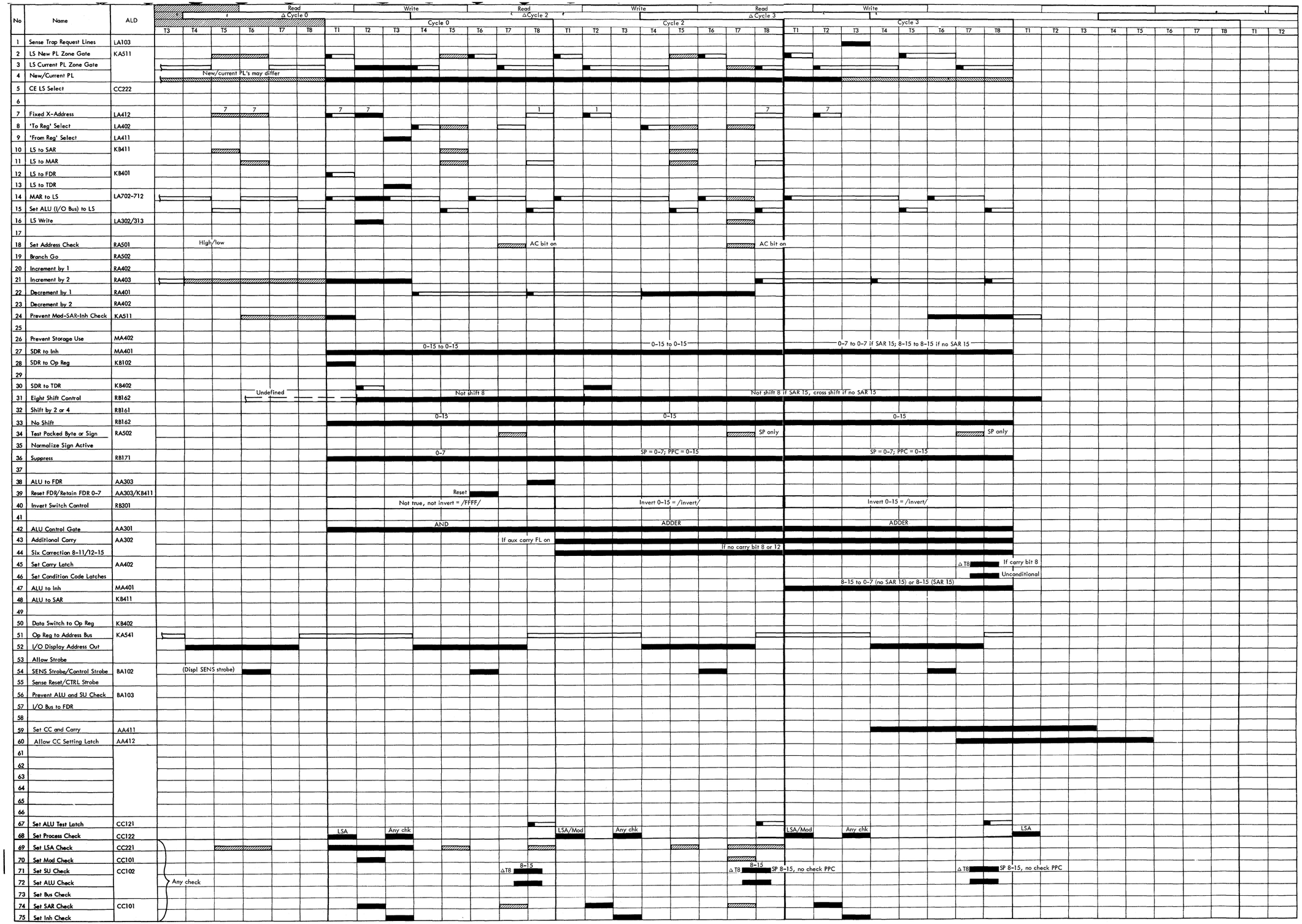
0 1 2 3 CC-latches

SP and PPC must be preceded by a control instruction which sets a previous carry (latch on) and sets the condition code to 1000 (result zero).

Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

Diagram 5-60. Subtract Packed Byte/Perform Packed Complement (XD) (Part 1 of 2) (03765) 2020 ≥ 50 090 FEMDM Vol 2 (8/69)

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59	Set CC and Carry	AA411
60	Allow CC Setting Latch	AA412
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle ▭ Cycle ▬

● **Diagram 5-60. Subtract Packed Byte/Perform Packed Complement (XD) (Part 2 of 2)** (03765A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

For SP, the two decimal digits in the byte address by the 'from reg' are subtracted from the two decimal digits in the byte addressed by the 'to reg'. The result is set into the byte addressed by the 'to reg'.

For PPC, the complement of the two decimal digits in the byte addressed by the 'from reg' is set into the byte addressed by the 'to reg'.

The 'from' byte remains unchanged.

A previous carry (aux carry latch on) is implemented in the operation.

Before initiating SP or PPC, the previous carry must be simulated by turning on the carry latch by a control /10/, bit 11, to obtain the correct complement.

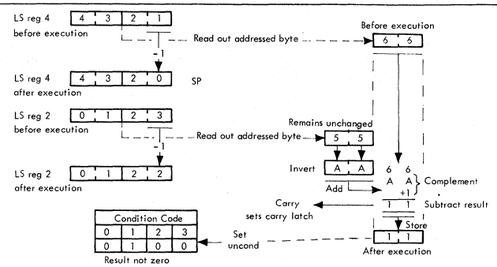
A carry out of the low-order byte turns on the carry latch. The condition code latches are set. A data check occurs when one of the operand bytes is not in packed decimal format.

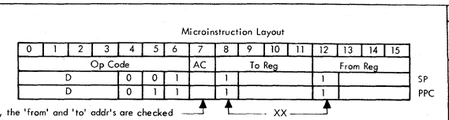
The 'from' and 'to' addresses are decremented by 1. If the AC bit (instruction bit 7) is on, an address check occurs when the 'from' or 'to' address is outside customer area.

The operation is performed in ALC mode when 'to reg' = 3 and 'from reg' = 5. Each operand has its own field length. The field length may be different. LS register 0 contains the field length of the 'from operand'. LS register 1 contains the field length of the 'to operand'.

The field length is the real number of bytes in an operand field reduced by 1.

The operand addresses are decremented by 1 every time one byte has been operated.





INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD GEB 0-1046-XXX
D3CA	SP	4I,2I,AC	CC,C/BY(R4,AC)+=PY(R4,-1),D-,PY(R?,AC,-1),D-,C
D7CA	PPC	4I,2I,AC	CC,C/BY(R4,AC,-1)+=PY(R4,AC,-1),D+,C
D3BD	SP	3I,5I,AC	CC,C/BY(R3,AC,UNTIL R1,LT,0)+=BY(R3,-1),D-,BY(R5,AC,-1, UNTIL R0,LT,0),D-,C

Mnemonic
SP
PPC
Format
FF
Type
XX (ALC)

Repeat Δ Cycle 1 – Δ Cycle 2 – Δ Cycle 3 — ALC end op — No / Yes → Δ Cycle 0

Δ Cycle 0 | Δ Cycle 1 | Δ Cycle 2 | Δ Cycle 3

Cycle 0 | Cycle 1 | Cycle 2 | Cycle 3

Read | Write | Read | Write | Read | Write | Read | Write

T1 T2 T3 T4 T5 T6 T7 T8 T1 T2 T3 T4 T5 T6 T7 T8 T1 T2 T3 T4 T5 T6 T7 T8 T1 T2 T3 T4 T5 T6 T7 T8 T1 T2 T3 T4 T5 T6 T7 T8 T1

No storage use if LC FL2 | No storage use if LC FL1 | Δ T8

CORE STORAGE

Read out and regenerate micro-instruction

SDR D 3 C A (7)

Op Reg D 3 C A (7)

SP PPC

Read out and regenerate 'from operand'

SDR 8 8 5 5

TDR 8 8 5 5

No / Yes — SAR 15

Packed byte — No

Data error FL — Force trap-req 2; PL switching after the current instr

SU

Suppress

0 0 5 5

5 5 0 0

AND

ALU

Invert sw

F F F F / F F F F

Read out and regenerate 'to operand'

SDR 7 7 6 6

TDR 7 7 6 6

No / Yes — SAR 15

Packed byte — No

SP SP PPC SP PPC

0 0 6 6 / 0 0 0 0

Not carry bit 12-8

If aux carry FL

+1 1 B -6

1 A -6

ADD

SP PPC

0 F / 0 F

F F A A Invert 0 0 5 5

ALU carry bit 8

Carry FL

FDR blank

Reset FDR

FDR 0 0 5 5

Read out 'to operand'

SDR 7 7 6 6

Data error FL — Force trap-req 2; PL switching after the current instr

Store halfword into position addressed by 'to reg'

Sense trap req

7 7 1 1 / 7 7 4 5

SAR 15 — No / Yes

1 1 / 4 5 SP PPC

Data error FL — Force trap-req 2; PL switching after the following instr

0 1 2 3 CC FL's

(LS reg 2) From Reg 0 1 2 3

MAR 0 1 2 3 -1

SAR 0 1 2 3 — SAR 15

From Reg 0 1 2 2

AC

LS Reg 0 0 0 0 A

MAR 0 0 0 A -1

LS Reg 0 0 0 0 9

ALC — No / Yes — No action

Decrement carry 0 turns on LC FL2

To Reg (LS reg 4) 4 3 2 1

MAR 4 3 2 1

SAR 4 3 2 1 — SAR 15

AC

LS Reg 1 0 0 0 C

MAR 0 0 0 C -1

LS Reg 1 0 0 0 B

ALC — No / Yes — No action

Decrement carry 0 turns on aux LC FL1→LC FL1

LC FL 1 and LC FL2 force end op ALC

(LS reg 4) To Reg 4 3 2 1

MAR 4 3 2 1 -1

SAR 4 3 2 1 — SAR 15

AC

To Reg 4 3 2 0

IAR 8 0 0 2

MAR 8 0 0 2 +2

IAR 8 0 0 4 (NSI, ALC)

ALC end op — No / Yes — No action

IAR 8 0 0 2

MAR 8 0 0 2 +2

IAR 8 0 0 4 (NSI)

ALC — No / Yes — No action

SAR 8 0 0 2

Condition Code	
1 0 0 0	Result is zero
0 1 0 0	Result is not zero
× × 0 1	Overflow

0 1 2 3 CC-latches

SP and PPC must be preceded by a control instruction which sets a previous carry (latch on) and sets the condition code to 1000 (result zero).

In ALC mode, further condition code setting is suppressed when a code other than zero is detected. ALC condition code can be result zero or not zero.

In ALC mode, overflow condition is set if the 'to field' length is smaller than the 'from field' length and the additional 'from' data is not all zero.

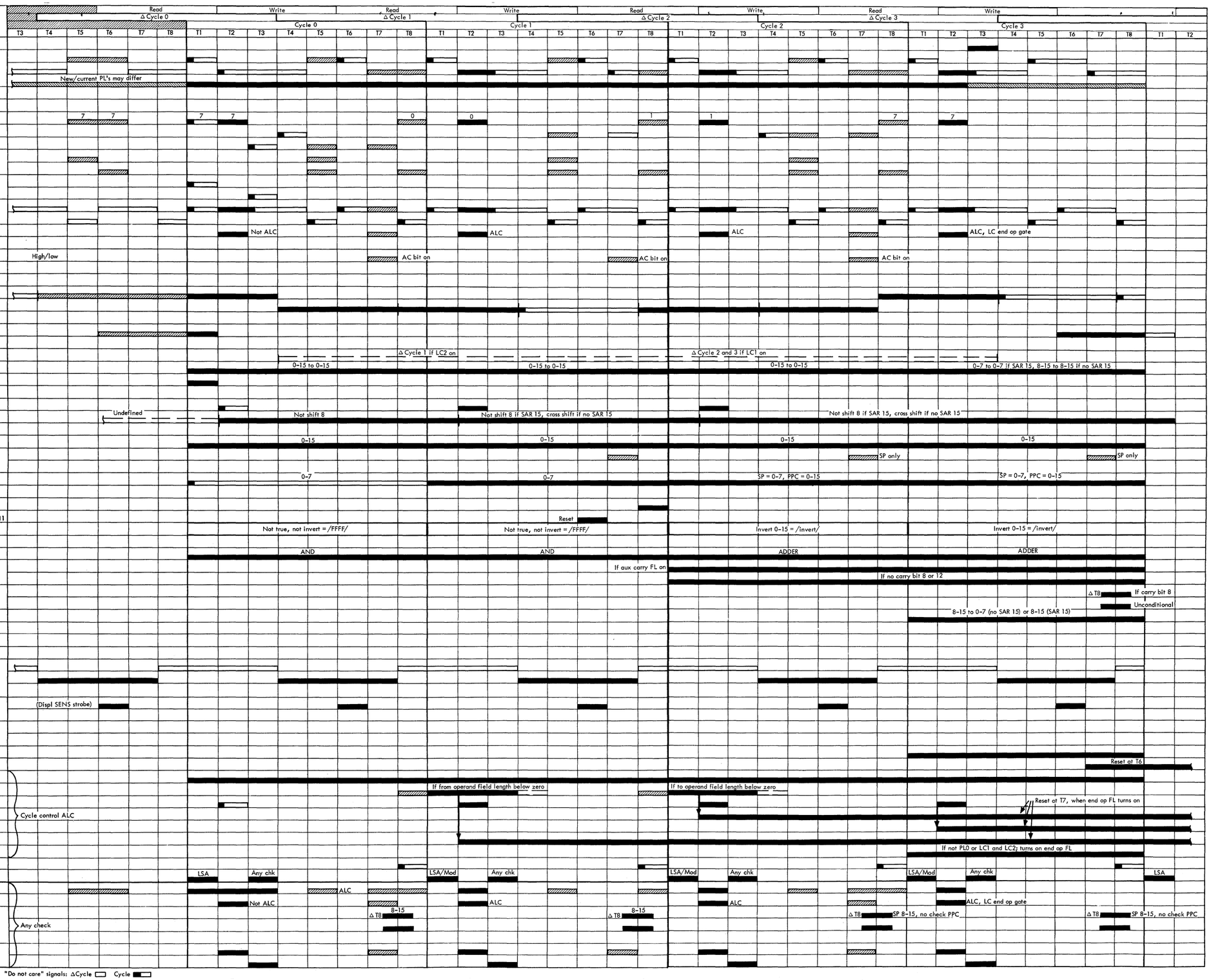
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle

Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

Diagram 5-61. Subtract Packed Byte/Perform Packed Complement (XX, ALC) (Part 1 of 2) (03766)

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58	Set CC and Carry	AA411
59	Allow CC Setting	AA412
60	Skip Cy 3 to Cy 1	KA411
61	Decrement Carry 0	RA301
62	Set LC (Latches)	KA414
63	Aux LC Latch 1	KA413
64	LC Latch 1	KA414
65	LC Latch 2	KA413
66	End Op Gate	KA412
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



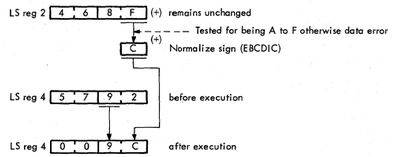
Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▭

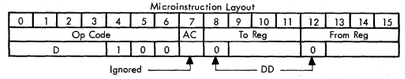
● Diagram 5-61. Subtract Packed Byte/Perform Packed Complement (XX, ALC) (Part 2 of 2) (03766A)

The packed decimal sign (low-order four bits) in the 'from reg' is translated into the standard sign according to the selected code. The code is selected by the USASCII latch (on = USASCII, off = EBCDIC). The USASCII latch can be turned on by a control/11/, bit 14, not bit 12; and it can be turned off by a control/11/, not bit 14, not bit 12.

The standardized sign is set into the low-order four bit position of the 'to reg'. The high-order four bit position of the low-order byte in the 'to reg' and the 'from reg' remain unchanged. The high-order byte of the 'to reg' is set to zero. 'From reg' and 'to reg' may be the same LS register. Address check is ignored.

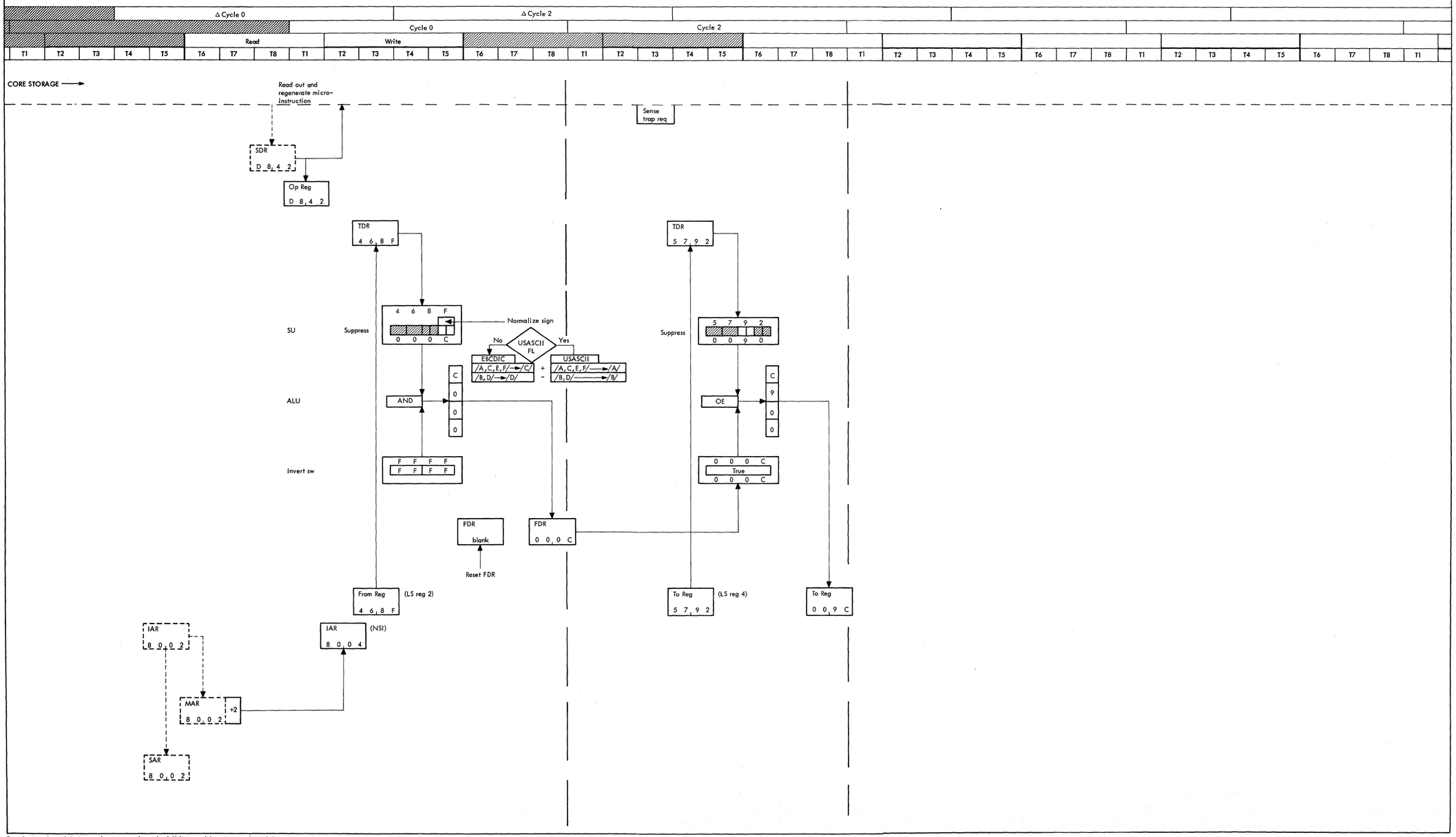
The sign is not checked for validity. If the sign pattern is invalid, the normalize function is inhibited. The invalid sign is set into the 'to reg'





Mnemonic
SDS
Format
FF
Type
DD

```
INST    MNEM  OPERANDS      STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
D842    SDS   ' 4,2         R4#=R4.0-11/R2.12-15 TEST FOR VALID SIGN AND NORMALIZE
```

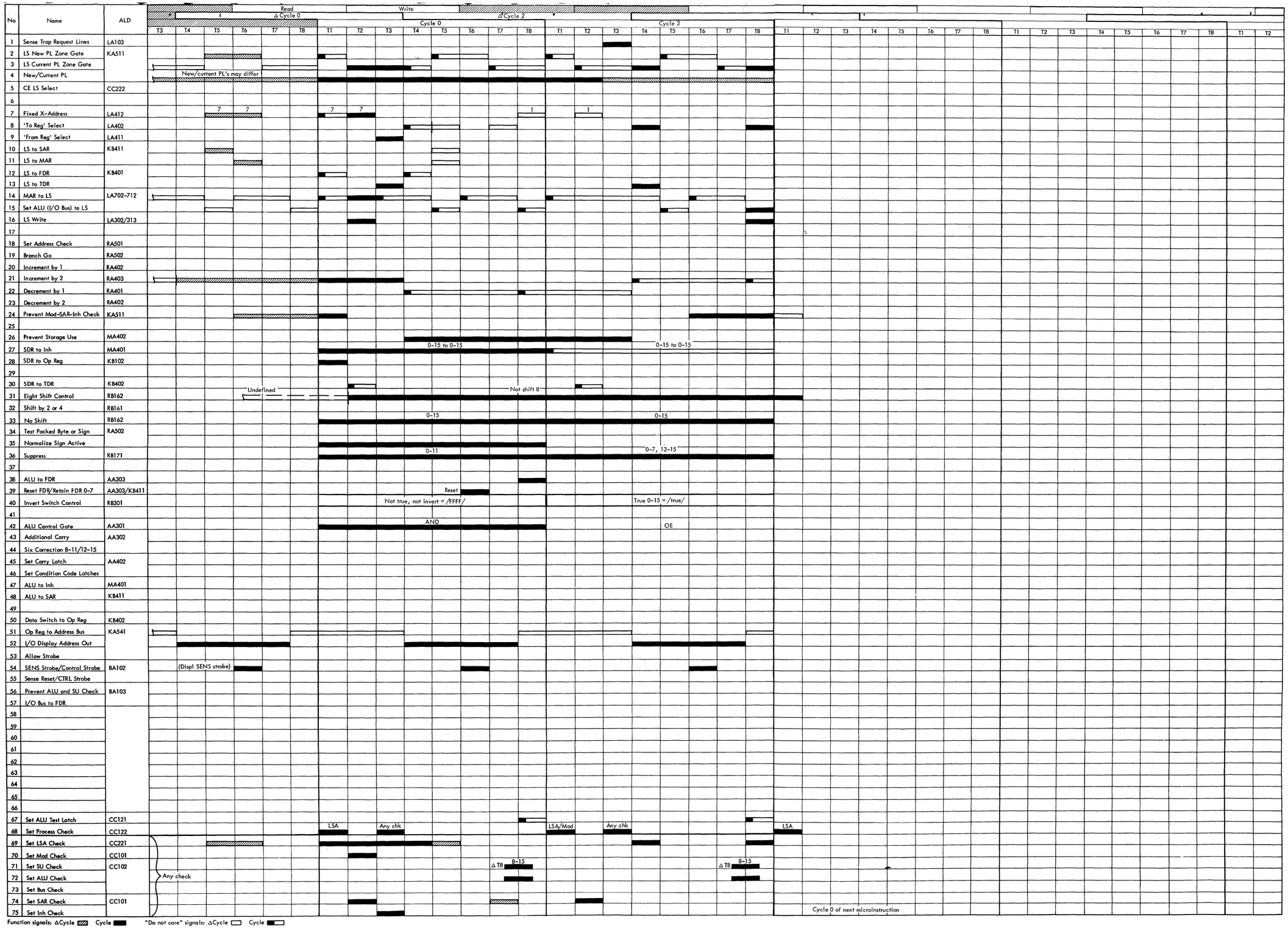


Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
Δ Cycle
Cycle

Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59		
60		
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▭

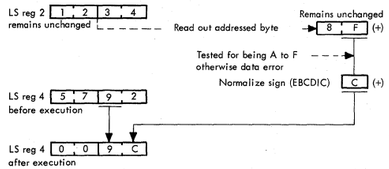
● Diagram 5-62. Set Decimal Sign (DD) (Part 2 of 2) (03767A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

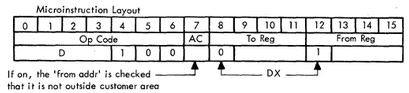
The packed decimal sign in the low-order four bit position of the byte addressed by the 'from reg' is standardized, according to the selected code, and set into the low-order four bits of the 'to reg'. The high-order four bits of the low-order byte in 'to reg' as well as the 'from' byte remain unchanged. The high-order byte in 'to reg' is set to zero.

If the AC bit (instruction bit 7) is on, an address check occurs when the 'from address' is outside customer area. The 'from address' is not updated.

The code is specified by the USASCII latch (on = USASCII, off = EBCDIC). The USASCII latch can be turned on by a control/11/, bit 14, not bit 12, and can be turned off by control /11/, not bit 14 and not bit 12.

The sign is not checked for validity. If the sign pattern is invalid, the normalize function is inhibited. The invalid sign is set into the 'to reg'



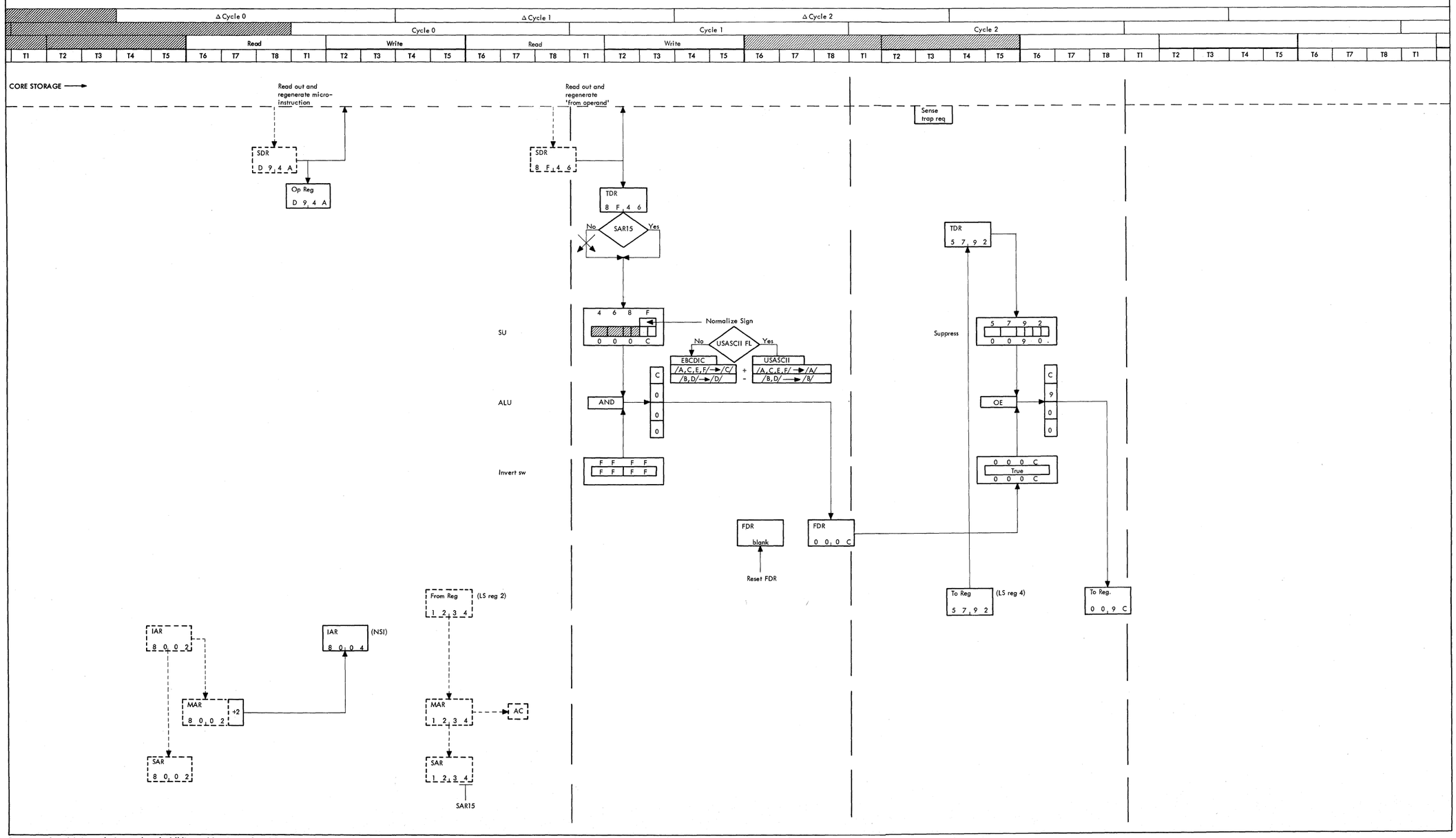


Mnemonic
SDS
Format
FF
Type
DX

```
INST    MNEM  OPERANDS     STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
D94A    SDS   4,2I,AC      R4+=R4.0-11/BY(R2,AC).4-7 TEST FOR VALID SIGN AND NORMALIZE
```

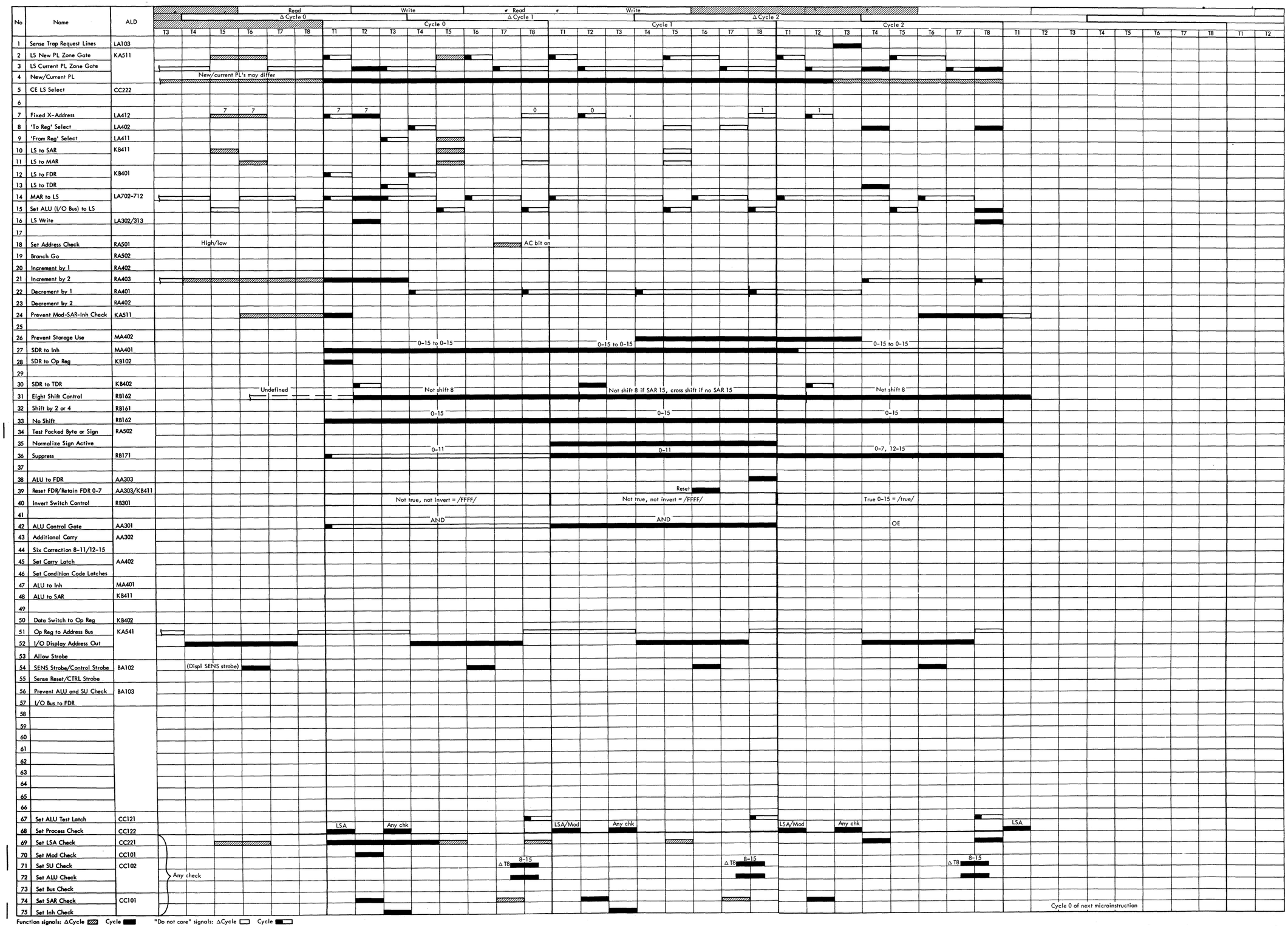
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59		
60		
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	

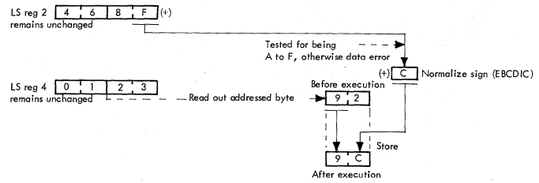


Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▭

The packed decimal sign in the low-order four bits of the 'from reg' is standardized according to the selected code and set into the low-order four bit position of the byte addressed by the "to reg". The high-order four bits of the 'to' byte as well as the 'from reg' remain unchanged. If the AC bit (instruction bit 7) is on, an address check occurs when the 'to address' is outside customer area. The 'to address' is not updated.

The code is specified by the USASCII (on = USASCII, off = EBCDIC). The USASCII latch can be turned on by a control/11/, bit 14, not bit 12, and can be turned off by a control 11/, not bit 14 and not bit 12.

A data check occurs when the low-order four bits in the from reg do not contain any hexadecimal value /A/ to /F/.



Microinstruction Layout

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Op Code							AC	To Reg				From Reg			
D		1	0	0			1					0			

If on, the 'to addr' is checked that it is not outside customer area

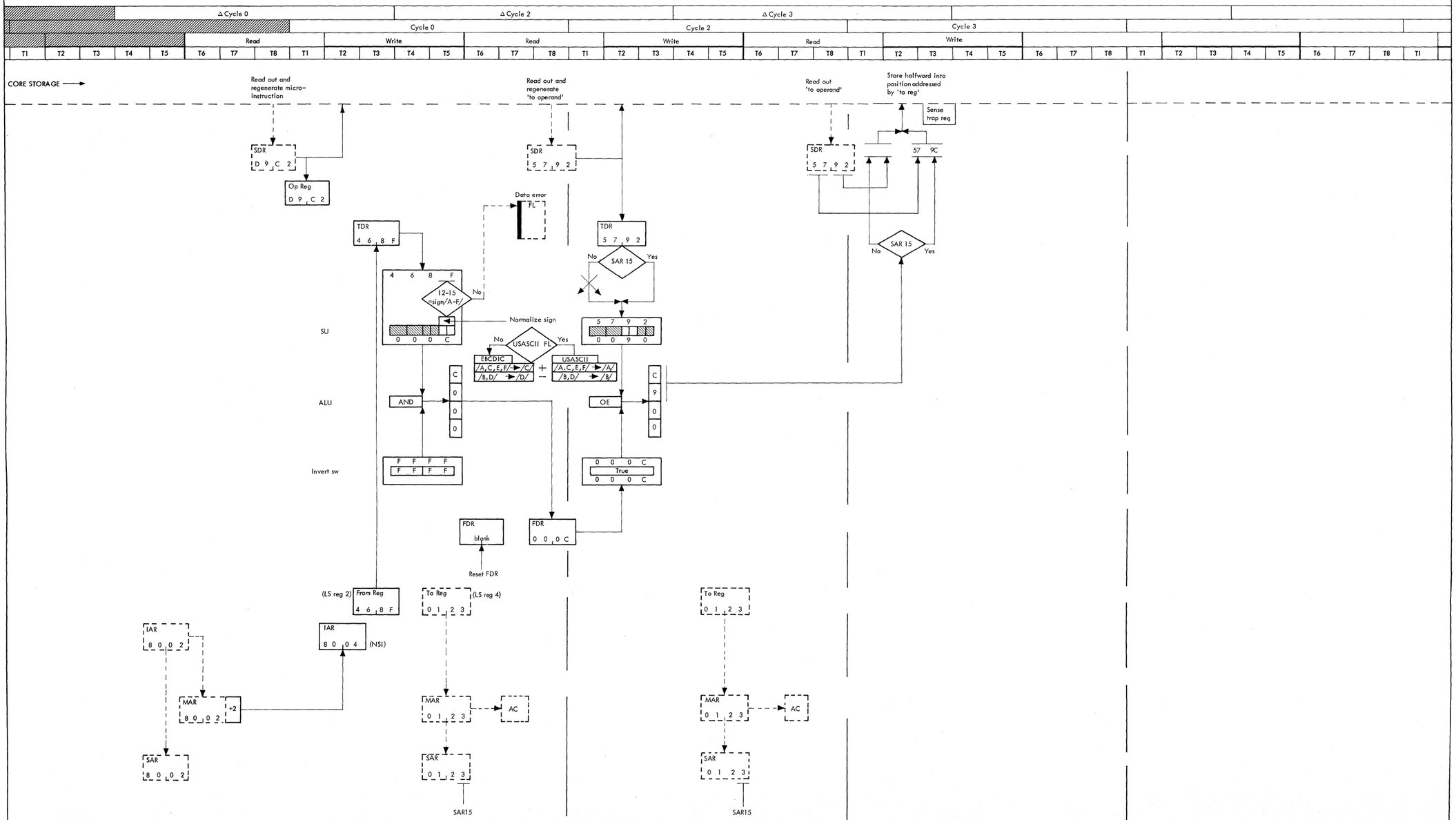
XD

Mnemonic
SDS
Format
FF
Type
XD

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
D9C2	SDS	4I,2,AC	BY(R4,AC).4-7*=R2.12-15 TEST FOR VALID SIGN AND NORMALIZE

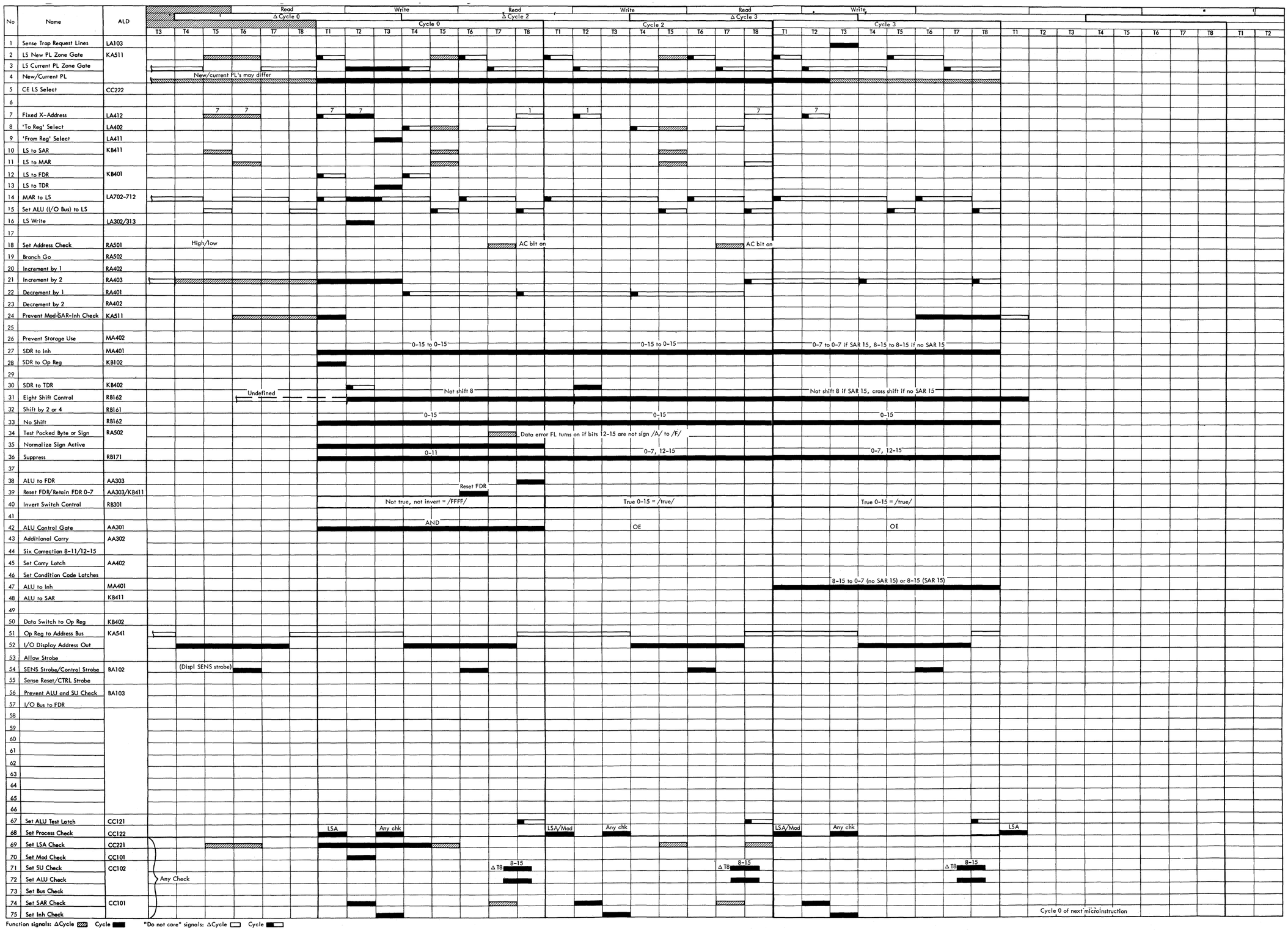
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59		
60		
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



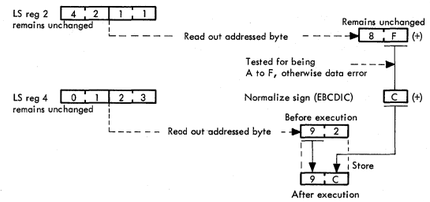
● Diagram 5-64. Set Decimal Sign (XD) (Part 2 of 2) (03769A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

The packed decimal sign in the four low-order bits of the byte addressed by the 'from reg' is standardized according to the selected code and set into the four low-order bits of the byte addressed by the 'to reg'. The four high-order bits of the 'to' byte as well as the 'from' byte remain unchanged. 'From reg' and 'to reg' may contain the same address or may be the same LS register

If the AC bit (instruction bit 7) is on, an address check occurs when one of the operand addresses is outside customer area. The operand addresses are not updated.

The code is specified by the USASCII latch (on = USASCII, off = EBCDIC). The USASCII latch can be turned on by a ctrl/11/, bit 14, not bit 12, and can be turned off by ctrl/11/, not bit 14 and not bit 12.

A data check occurs when the four low-order bits of the 'from' byte do not contain any hexadecimal value /A/ to /F/

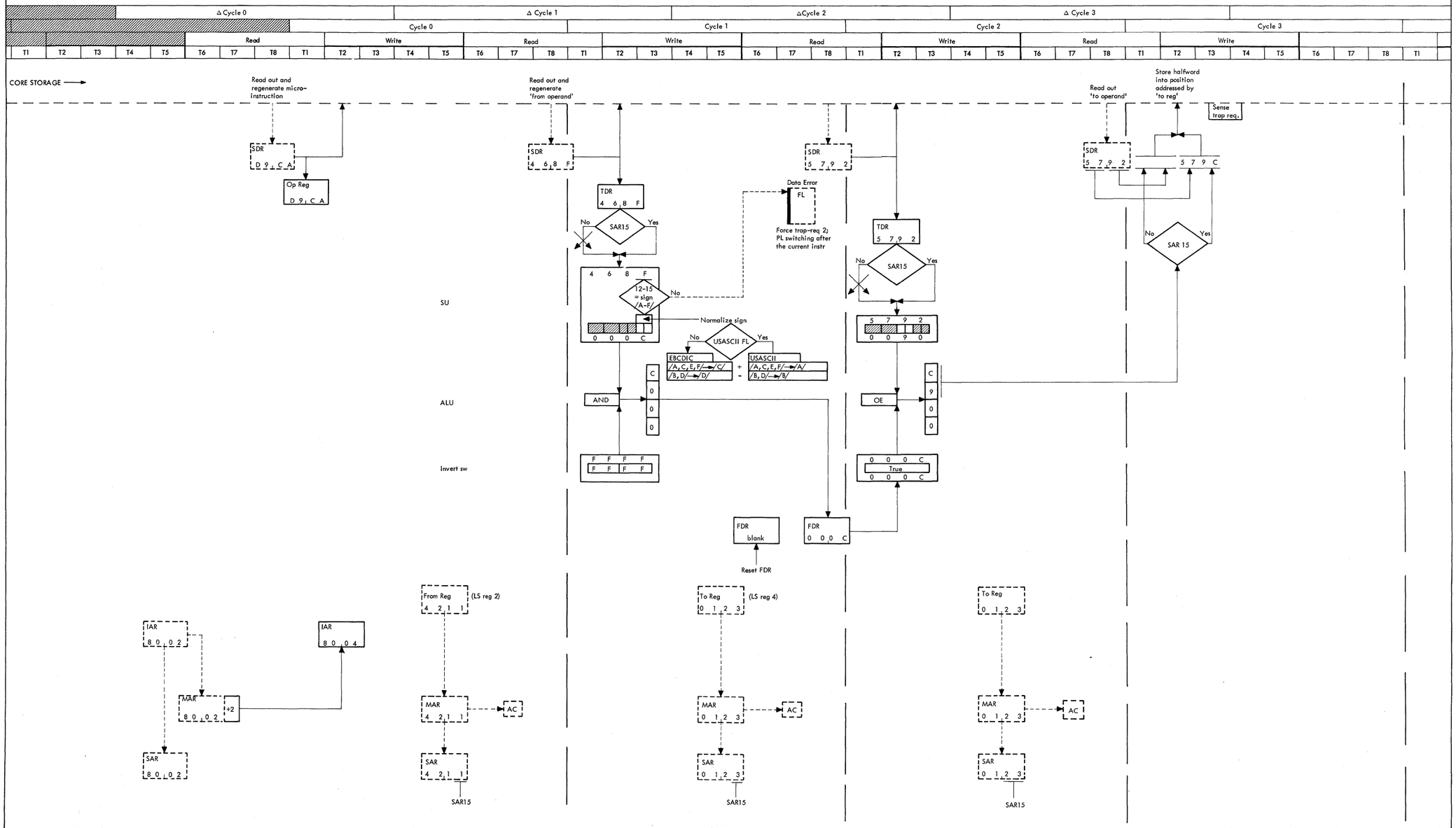


Microinstruction Layout

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Op Code							AC	To Reg				From Reg			
D				1	0	0	1	XX				1			

If on, the 'from' and 'to' addr's are checked that they are not outside customer area

Mnemonic
SDS
Format
FF
Type
XX

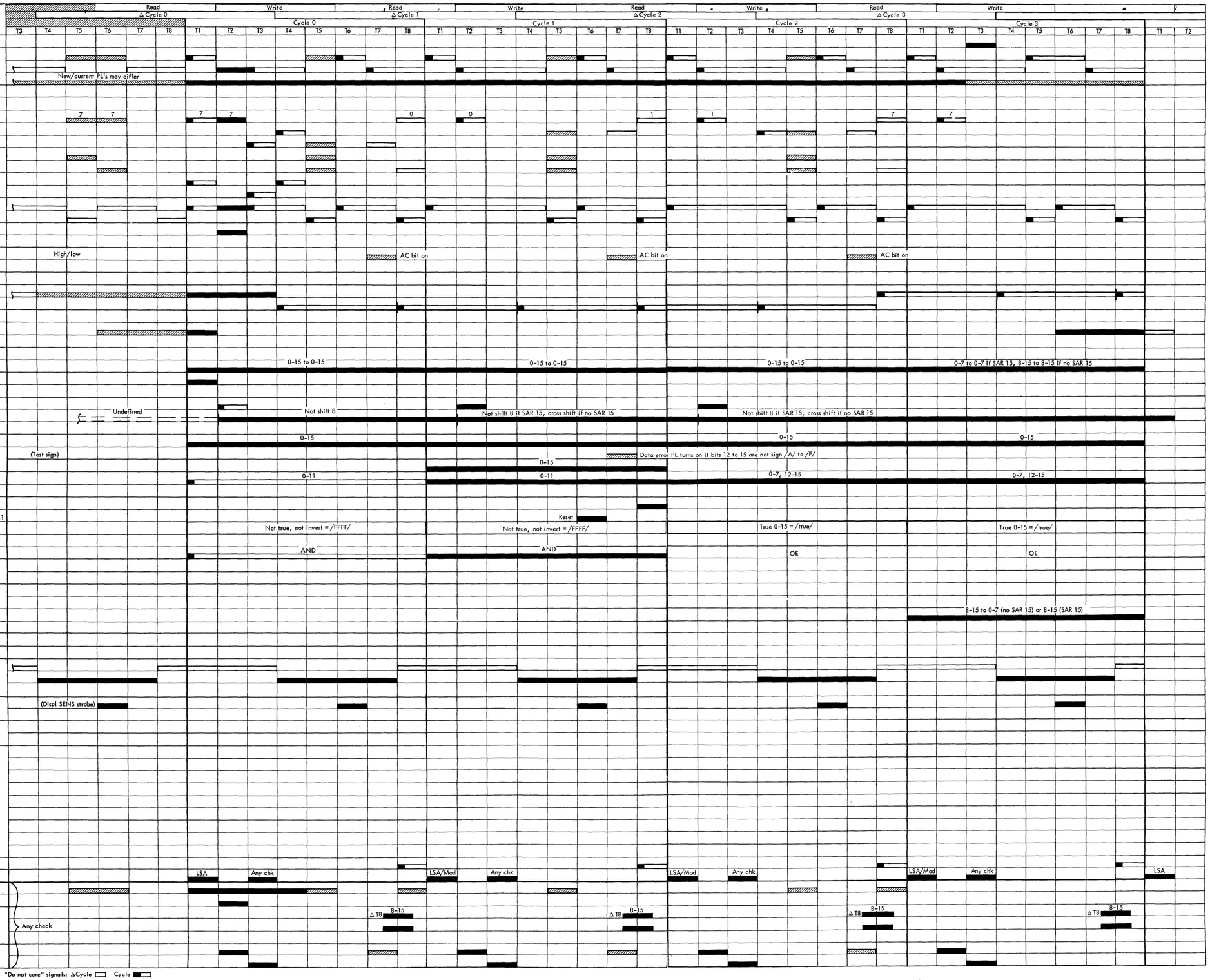


Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle

Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59		
60		
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▬

● Diagram 5-65. Set Decimal Sign (XX) (Part 2 of 2) (03770A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

The CPU stops after executing the instruction. The 'from reg' is displayed in data register P, I, U, L. The 'to reg' is displayed in data register E, S, T, R. The CPU can be started again by operating the start key. The next microinstruction to be executed will be that addressed by the updated IAR (HALT instruction address + 2).

LS reg 4 [1 2 3 4] remains unchanged

LS reg 2 [A B C D] remains unchanged

Display

P	I	U	L	E	S	T	R
A	B	C	D	1	2	3	4

CPU stops

Microinstruction Layout

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Op Code								To Reg			From Reg				
D			1	1	0	0	0				0				

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
DC42	HALT	4,2	FDR=E,S,T,R+=R4, TDR=P,I,U,L+=R2

Mnemonic
HALT
Format
FF
Type

Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
- △Cycle
- Cycle

△Cycle 0

Cycle 0

Read | Write

T1 T2 T3 T4 T5 T6 T7 T8 T1 T2 T3 T4 T5 T6 T7 T8 T1 T2 T3 T4 T5 T6 T7 T8 T1 T2 T3 T4 T5 T6 T7 T8 T1 T2 T3 T4 T5 T6 T7 T8 T1 T2 T3 T4 T5 T6 T7 T8 T1

CORE STORAGE

Read out and regenerate micro-instruction

SDR D C 4 2

Op Reg D C 4 2

TDR A B C D

SU

A B C D
A B C D

P I U L

E S T R

Display retained during CPU stop

1 2 3 4
True
1 2 3 4

Invert sw

FDR 1 2 3 4

CPU stop

(LS reg 2) From Reg A B C D

IAR 8 0 0 4 (NSI)

To Reg 1 2 3 4 (LS reg 4)

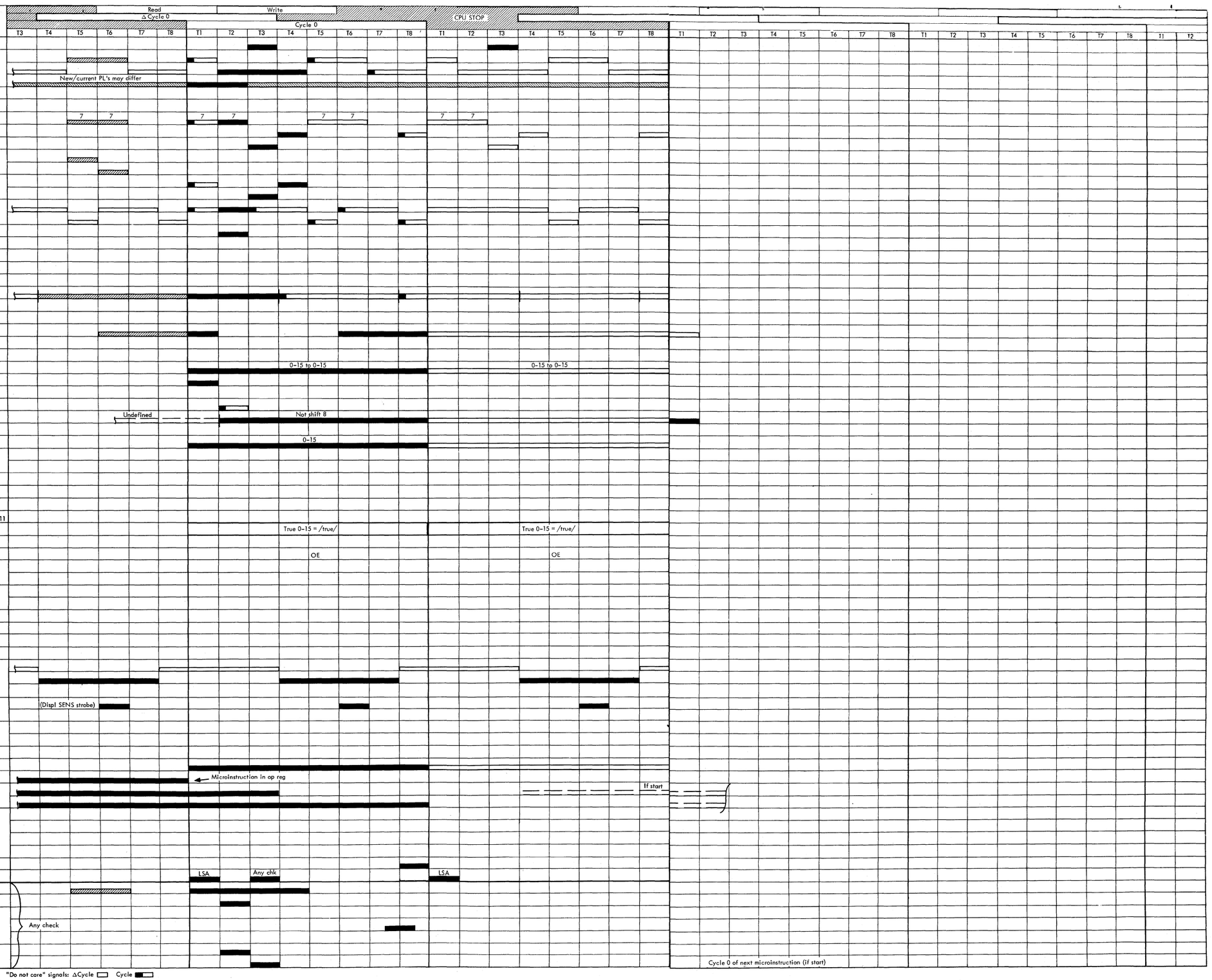
IAR 8 0 0 2

MAR 8 0 0 2 +2

SAR 8 0 0 2

Functions performed during cycle time are shown by full lines and functions performed during △ cycle time are shown by dotted lines.

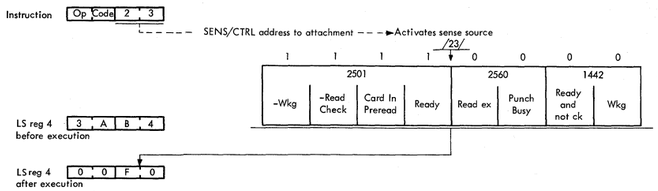
No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59	End Op Cycle 0	KA403
60	Hold Run Condition	KA521
61	Delta Process Latch	KA303
62	Process Latch	
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



● **Diagram 5-66. Halt and Display Halfword (Part 2 of 2)** (03771A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

A byte or halfword provided by a sense source (CPU or attachment) is set into 'to reg'. The sense source is selected by the SENS/CTRL address in the low-order byte of the instruction (256 different sources are possible). The SENS/CTRL address is set on the address bus. The sense byte is set on the data bus in the attachment to which the current SENS/CTRL address is co-ordinated. Except for the halfword SENS's (SENS/CTRL addresses /14/ and /15/), the

SENS/CTRL address on the returning address bus is exclusive ORed with the original SENS/CTRL address in the instruction. If both addresses are identical the result is zero. The result is set into the high-order byte of the 'to reg'.



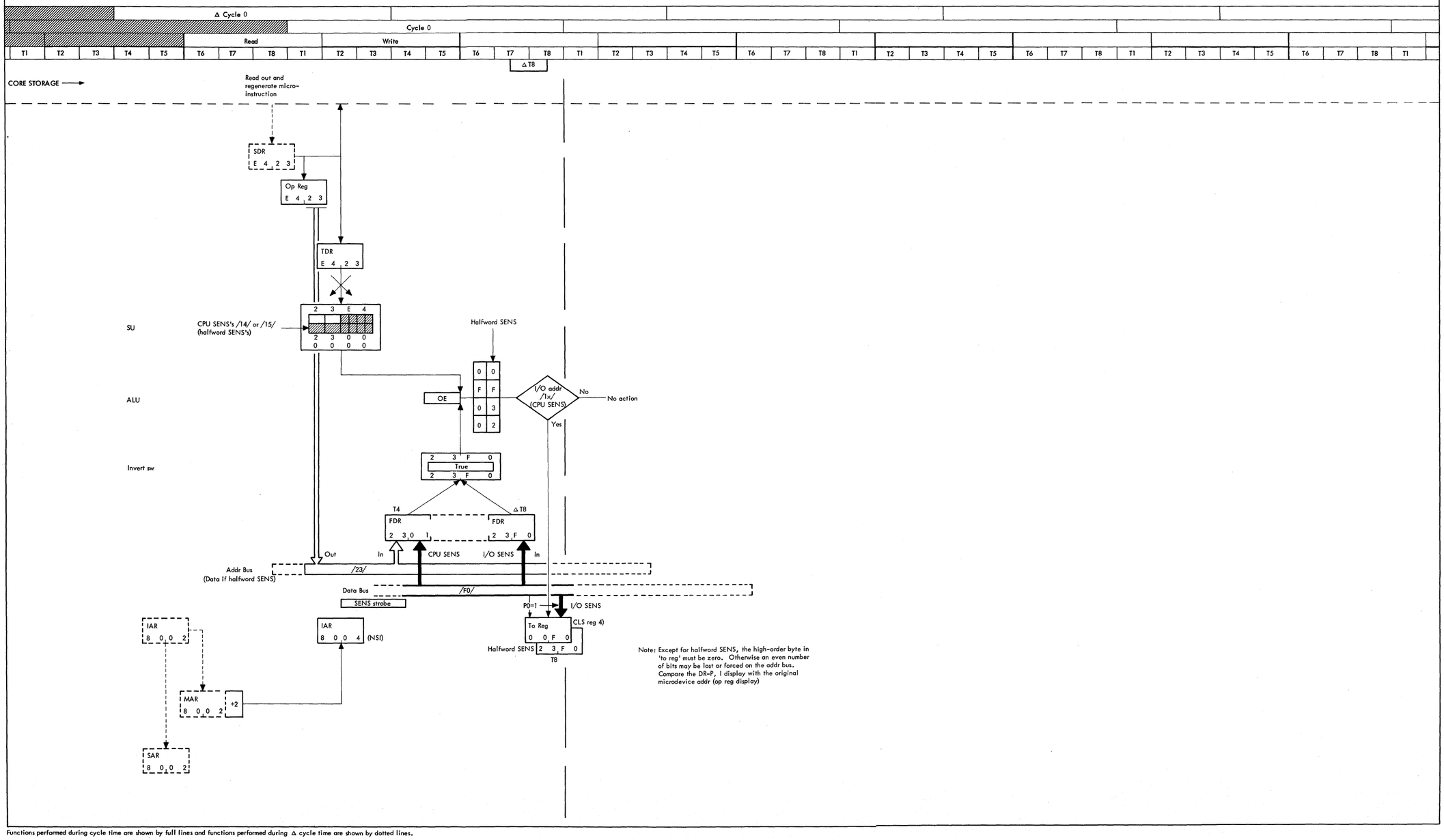
Microinstruction Layout

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Op Code				To Reg				SENS/Ctrl Addr							
E				0											

direct addressing

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
E423	SENS	4,X'23'	R4 * = '00'/SENSE 23

Mnemonic
SENS
Format
I/O
Type
Direct Addressing



Note: Except for halfword SENS, the high-order byte in 'to reg' must be zero. Otherwise an even number of bits may be lost or forced on the addr bus. Compare the DR-P, I display with the original microdevice addr (op reg display)

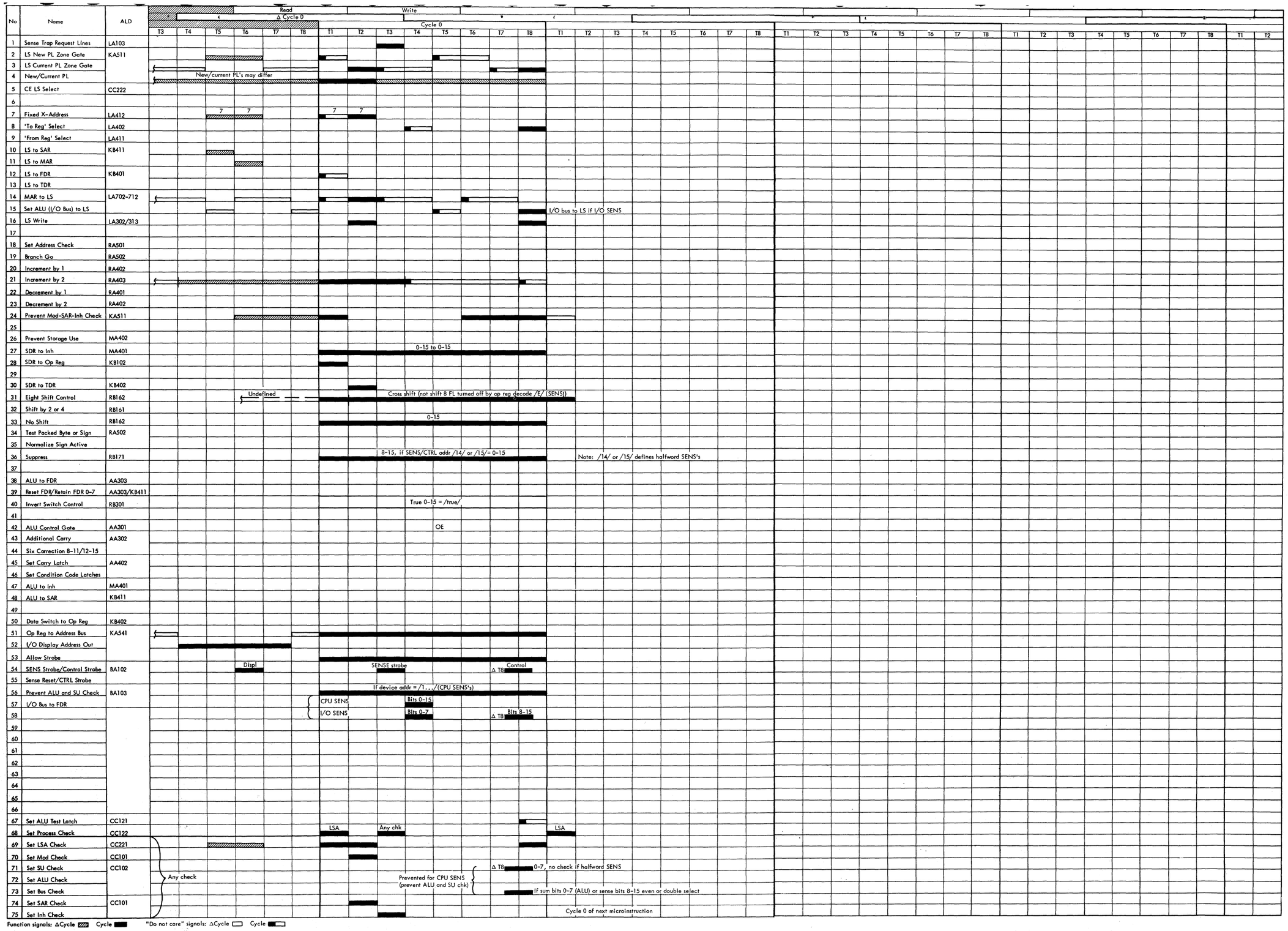
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle

Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

Diagram 5-67. SENS CPU I/O (Direct Addressing) (Part 1 of 2) (03772A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

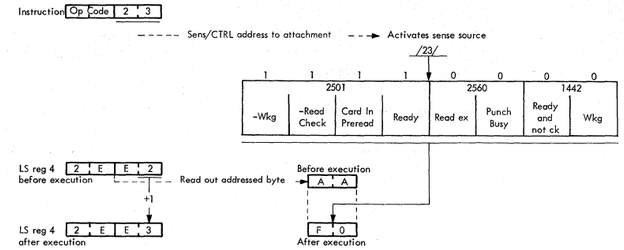
No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59		
60		
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	

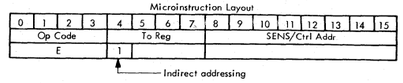


Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▭

● **Diagram 5-67. SENS CPU I/O (Direct Addressing) (Part 2 of 2)** (03772A)

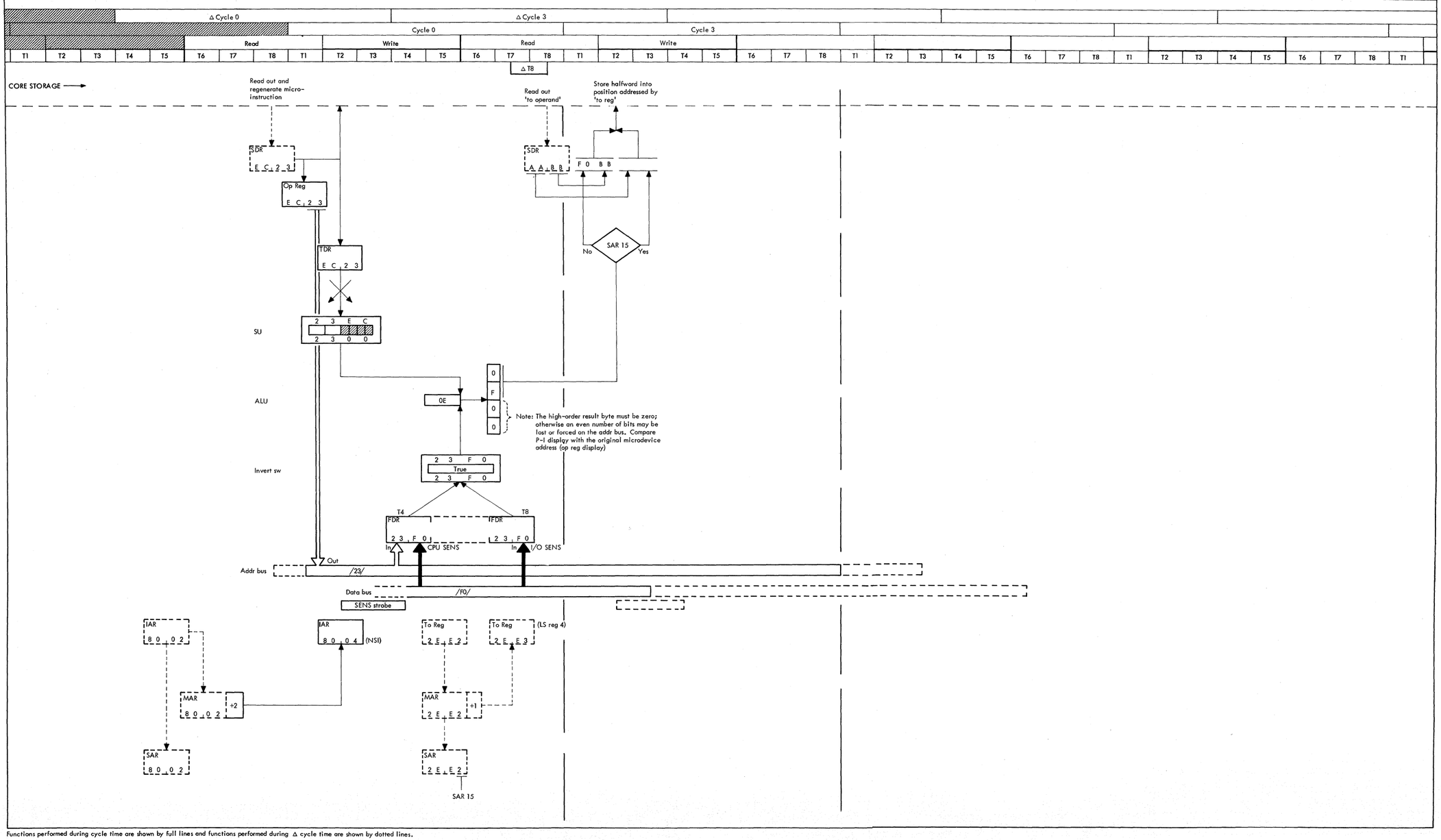
A byte provided by a sense source (CPU or attachment) is stored into the byte addressed by the 'to reg'. The 'to address' is incremented by 1. The sense source is selected by the SENS/CTRL address in the low-order byte of the instruction (256 different sources are possible). The SENS/CTRL address is set on the address bus. The sense byte is set on the data bus in the attachment to which the current SENS/CTRL address is co-ordinated. The SENS/CTRL address on the returning address bus is exclusive ORed with the original SENS/CTRL address in the instruction. If both addresses are identical the result is zero. The result can be displayed in the high-order ALU byte.





INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
EG23	SENS	4I,X'23'	BY(R4,+1) *= SENSE 23

Mnemonic
SENS
Format
I/O
Type
Indirect Addressing



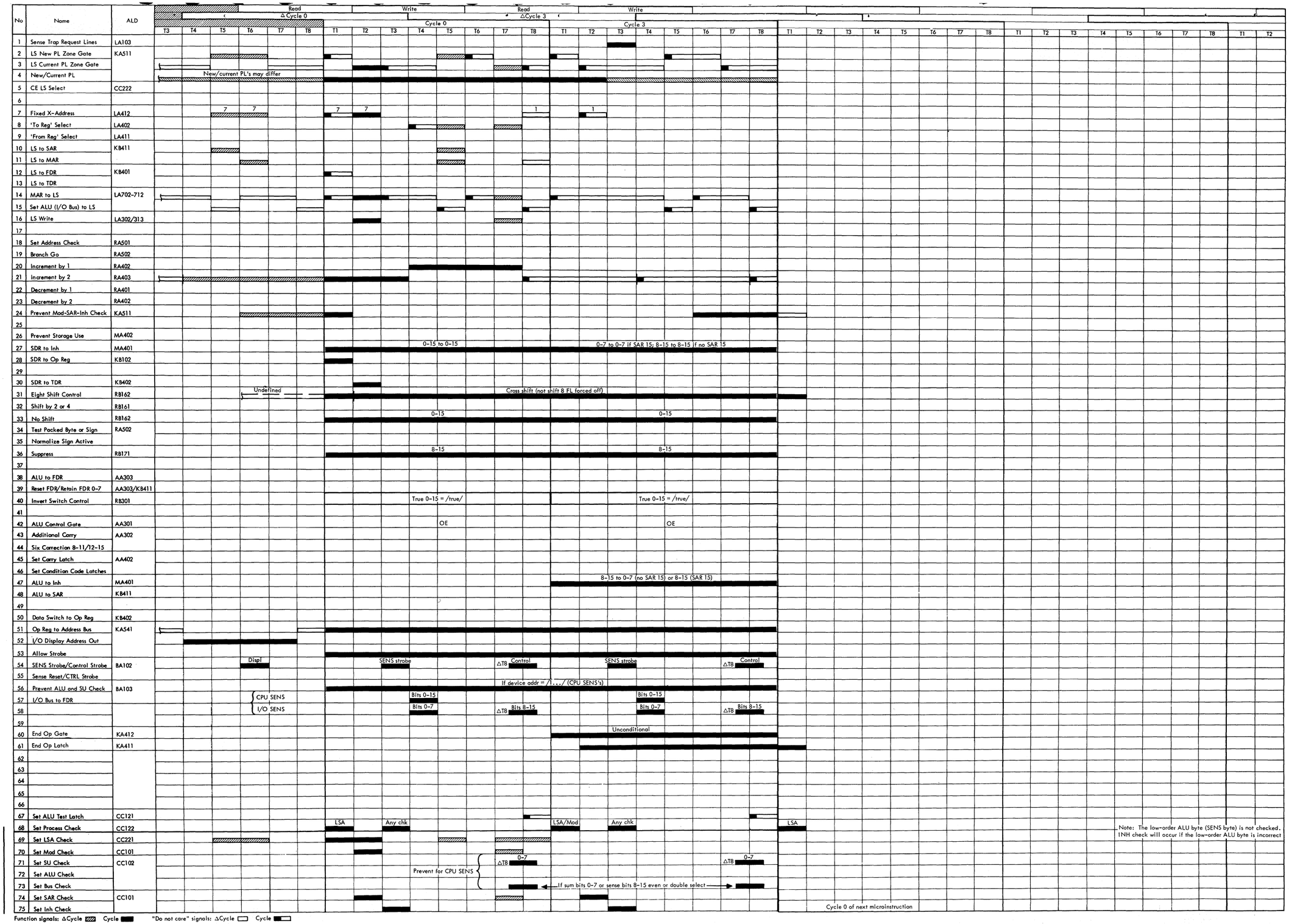
Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle

Diagram 5-68. SENS CPU I/O (Indirect Addressing) (Part 1 of 2) (03773A) 2020-2-50,000 EEMDM Vol 2 (8/69)

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59		
60	End Op Gate	KA412
61	End Op Latch	KA411
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▭

● **Diagram 5-68. SENS CPU I/O (Indirect Addressing) (Part 2 of 2)** (03773A)

If the 'to reg' field contains /7/ (111), an indirectly addressed SENS (see Diagram 5-69) is executed in ALC mode. LS register 1 contains the field length (real number of bytes to be sensed reduced by 1). LS register 6 contains the address of the byte into which the first sense byte must be stored. The field length is decremented by 1, and the store address is incremented by 1, every time a sense byte is stored.

This SENS ALC can be used to question a sense source with a repetition rate of 2 microseconds (diagnostic applications, ICR).

Microinstruction Layout

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Op Code				To Reg				SENS/Ctrl Addr							
E				1	1	1	1								

ALC

Mnemonic
SENS
Format
I/O
Type
ALC

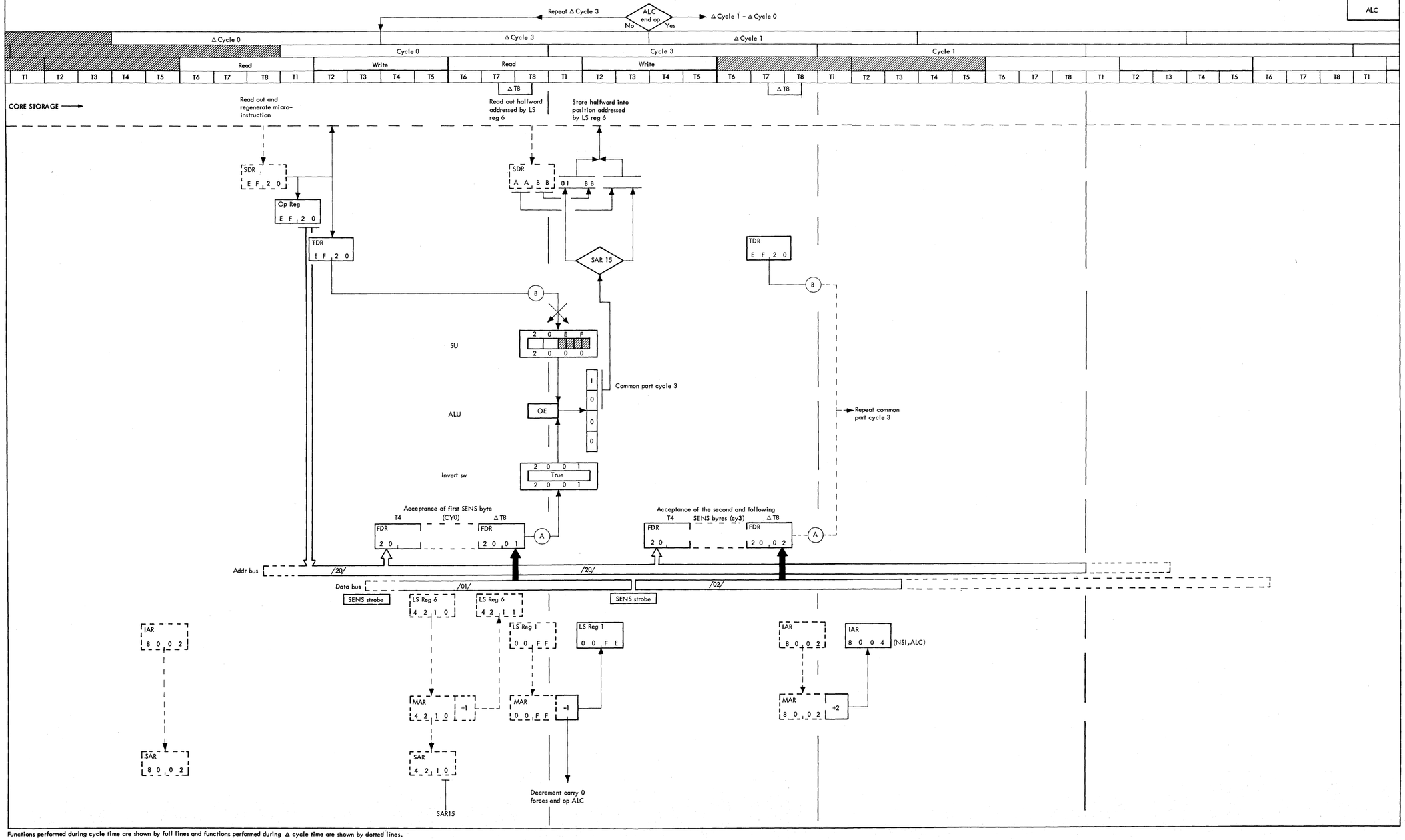
INST EF20 MNEM SENS OPERANDS 7I,X'20'

STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX

BY(R6,+1, UNTIL R1, LT, 0)*= SENSE 20

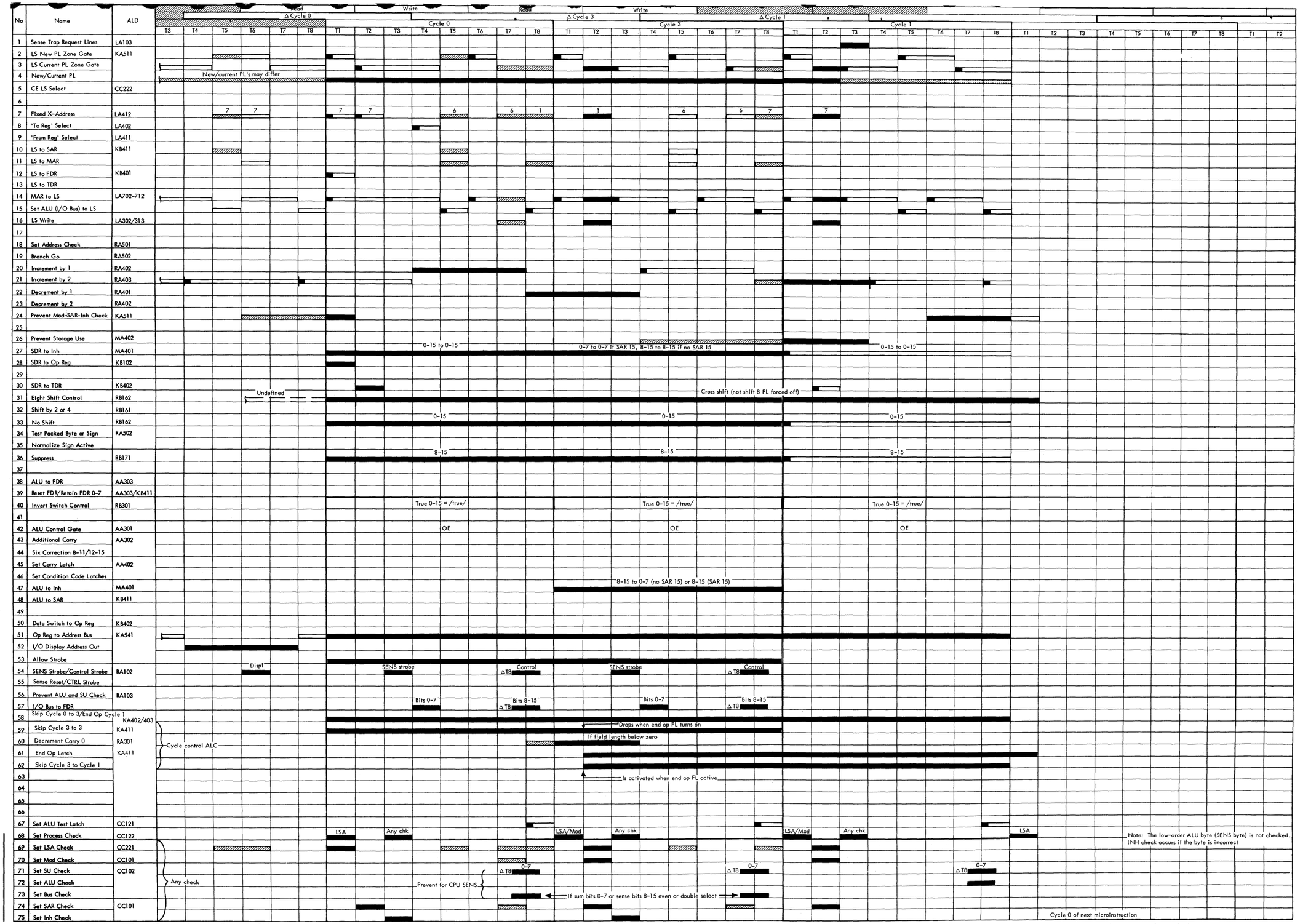
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58	Skip Cycle 0 to 3/End Op Cycle 1	KA402/403
59	Skip Cycle 3 to 3	KA411
60	Decrement Carry 0	RA301
61	End Op Latch	KA411
62	Skip Cycle 3 to Cycle 1	
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



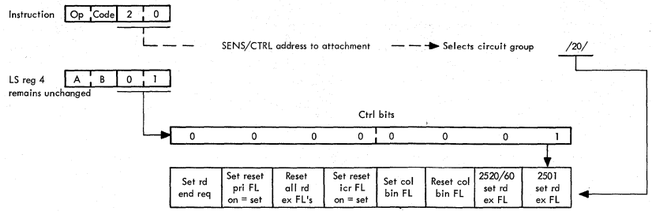
Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▭

● **Diagram 5-69. SENS I/O (ALC) (Part 2 of 2)** (03774A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

The low-order byte in 'to reg' is set onto the DATA BUS. The SENS/CTRL address (low-order byte of the instruction) is set on the address bus and selects the circuit group (in CPU or attachment) which shall be controlled according to the CTRL data on the data bus. The 'to reg' remains unchanged.

The returning address and data bus are set into FDR for display (E-S = returning SENS/CTRL addr, T-R returning ctrl data) if the CPU stops after the instruction.

The data bus output is displayed in U-L.



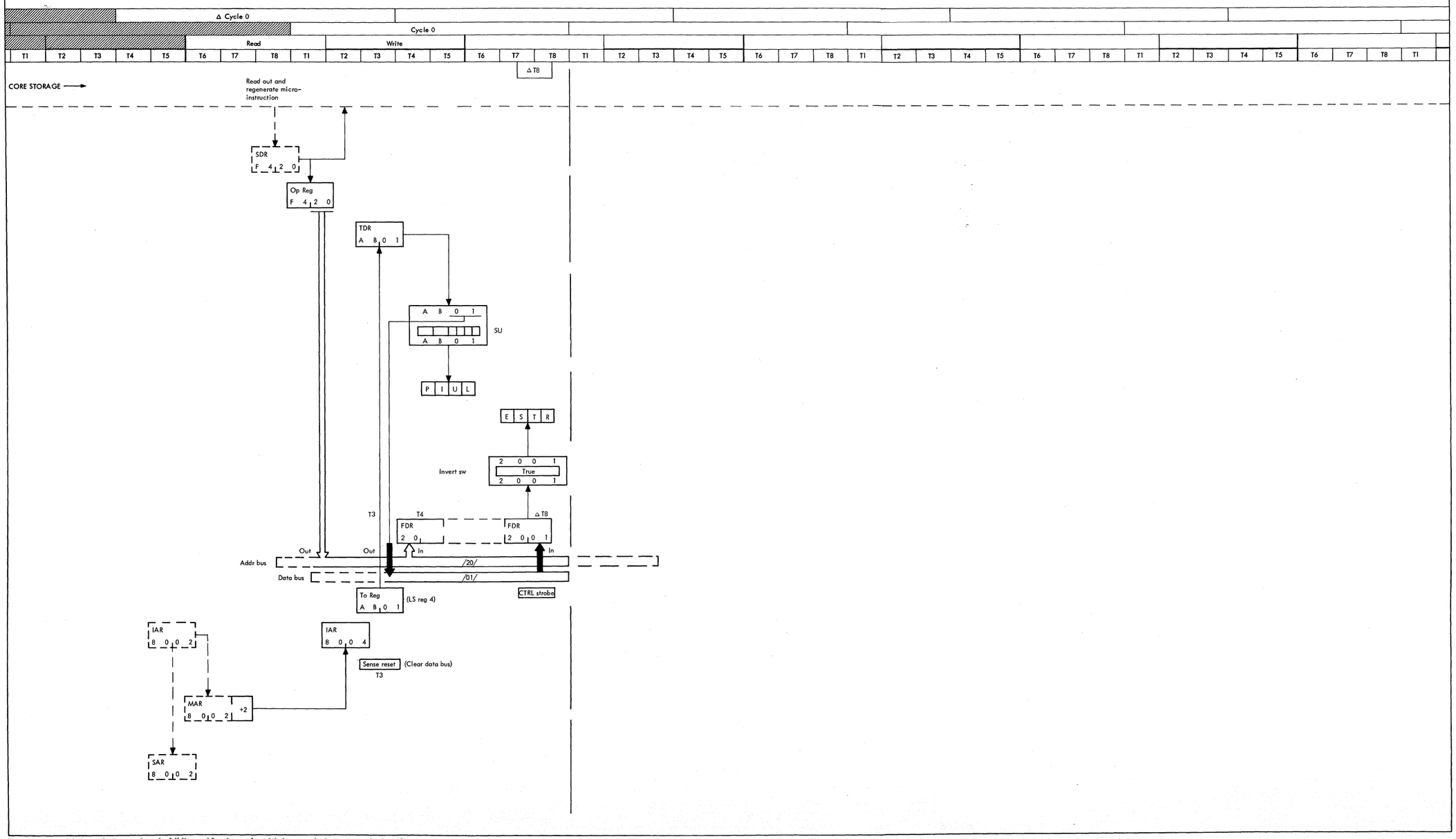
Microinstruction Layout

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Op Code				To Reg				SENS/Ctrl Addr							
F				0											

Direct addressing

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
F'420	CTRL	4,X'20'	CONTROL 20/R4.8-15

Mnemonic
CTRL
Format
I/O
Type
Direct Addressing



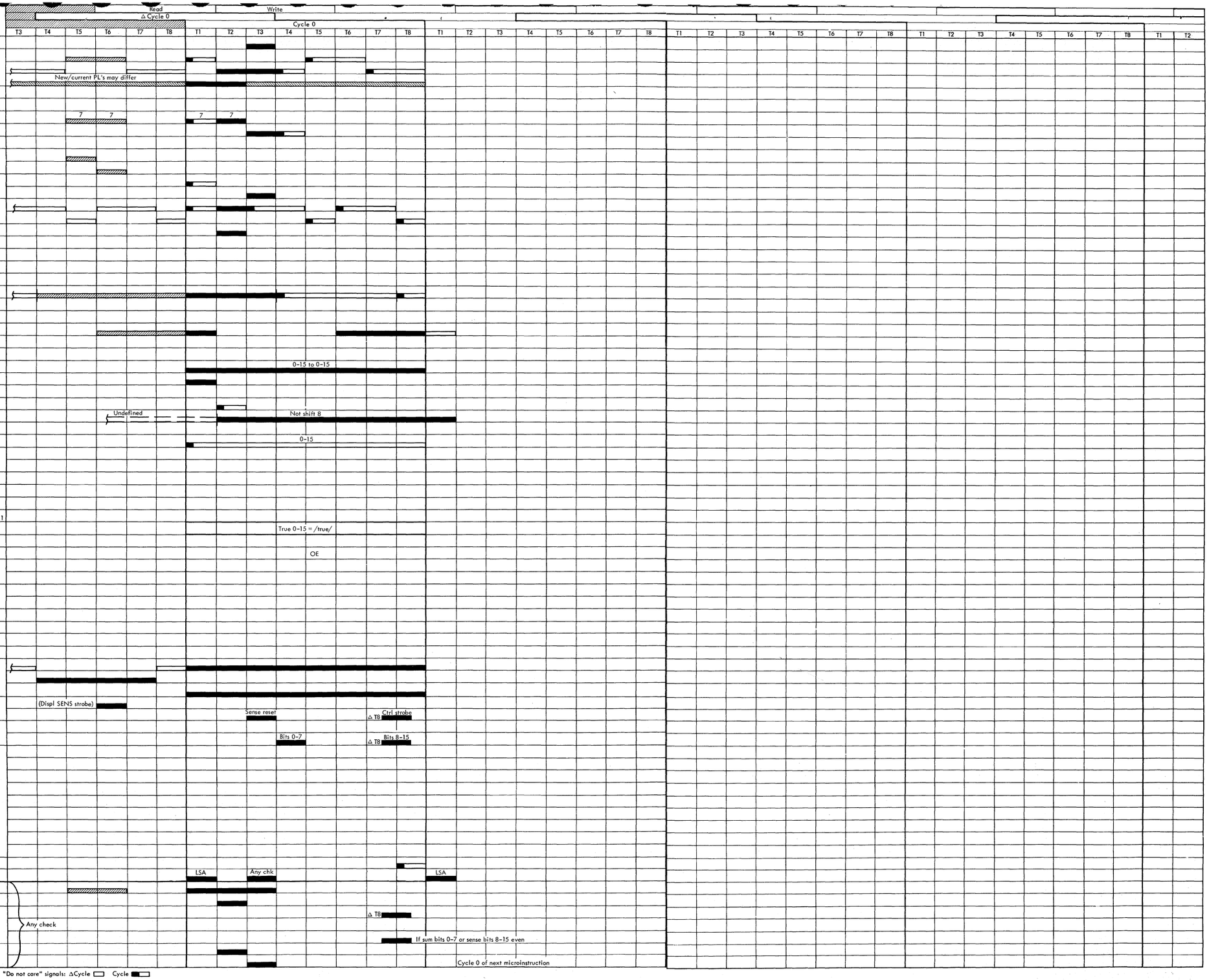
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle

Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

Diagram 5-70. Control I/O (Direct Addressing) (Part 1 of 2) (03775A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59		
60		
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



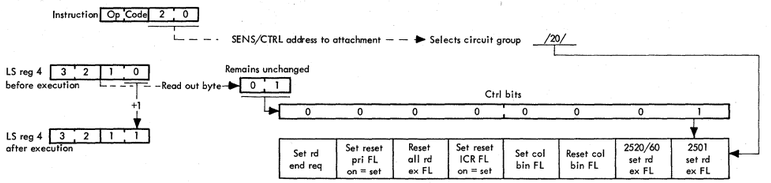
Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▭

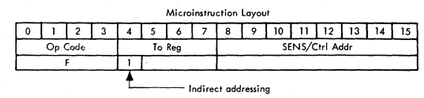
● Diagram 5-70. Control I/O (Direct Addressing) (Part 2 of 2) (03775A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

The byte addressed by the 'to reg' is set onto the data bus. The SENS/CTRL address (low-order byte of the instruction) is set on the address bus and selects the circuit group (in CPU or attachment) which shall be controlled according to the CTRL data on the data bus. The 'to' byte remains unchanged. The 'to' address is incremented by 1.

The returning address and data bus are set into FDR for display (E-S = returning SENS/CTRL addr, T-R returning CTRL data) if the CPU stops after the instruction.

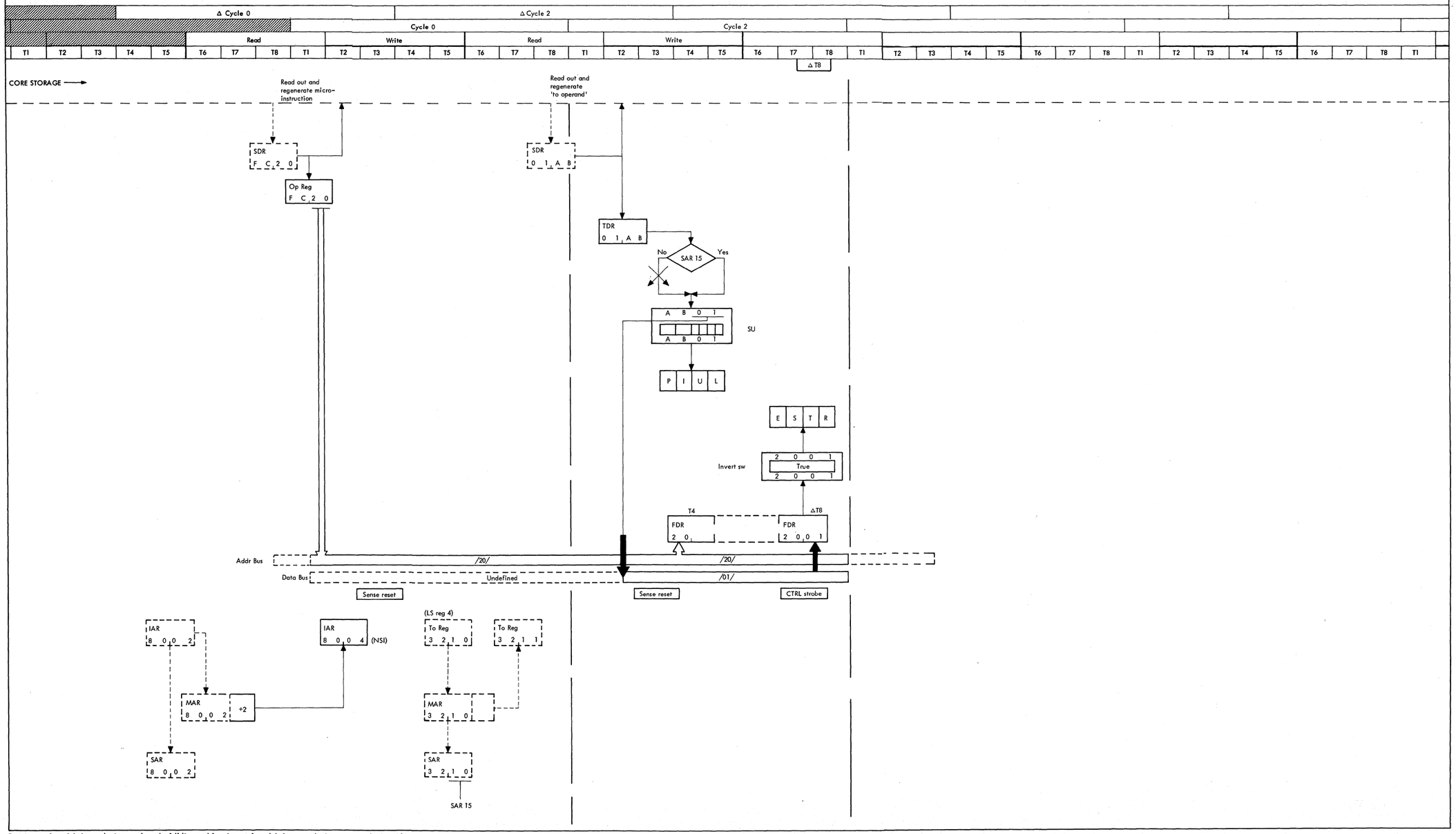
The data bus output is displayed in U-L.





INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
FC20	CTRL	4I,X'20'	CONTROL 20/BY(R4,+1)

Mnemonic
CTRL
Format
I/O
Type
Indirect Addressing



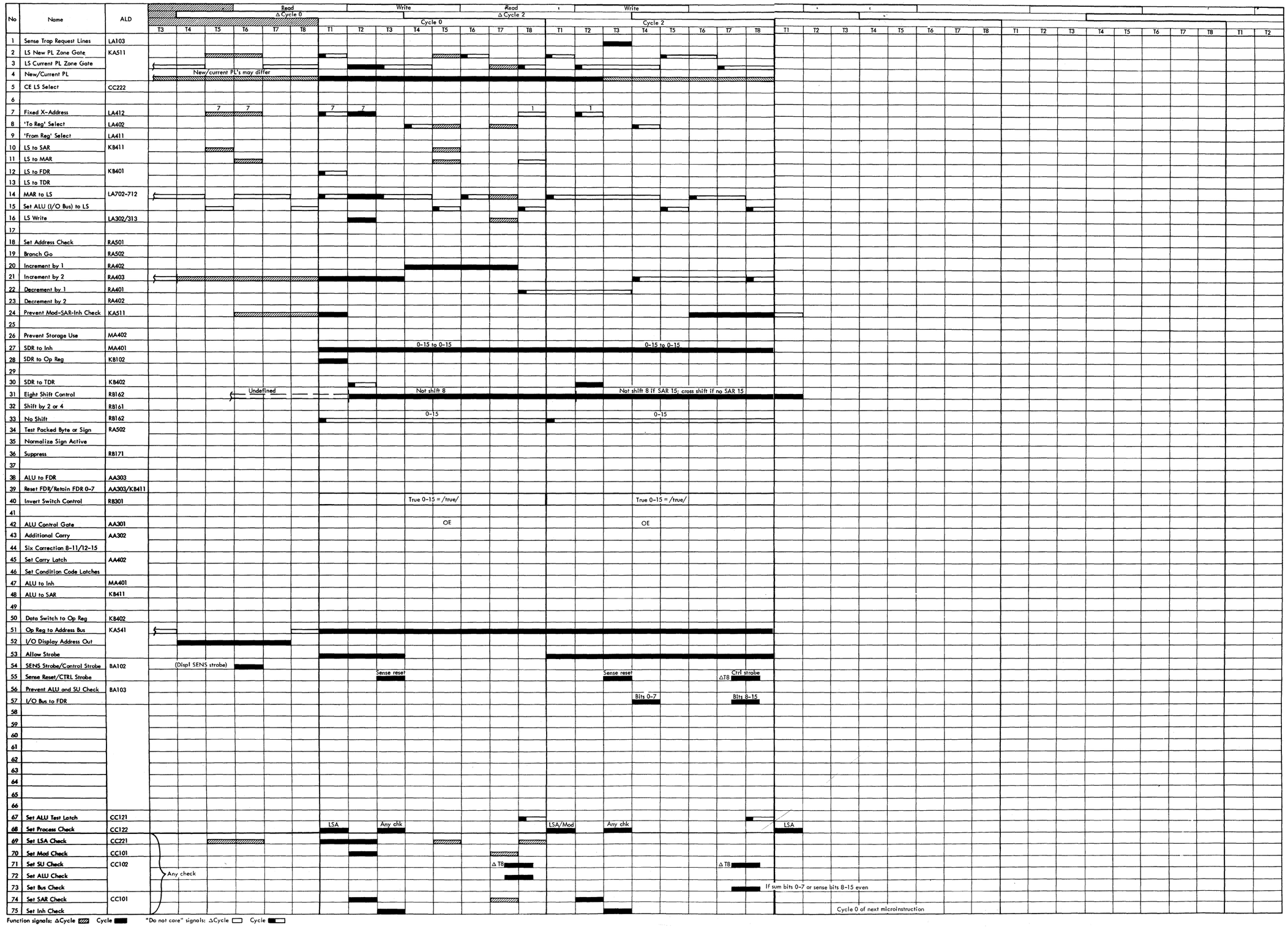
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle

Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

Diagram 5-71. Control I/O (Indirect Addressing) (Part 1 of 2) (03776A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59		
60		
61		
62		
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



Function signals: ΔCycle Cycle "Do not care" signals: ΔCycle Cycle

The indirect addressed ctrl (see Diagram 5-71) is executed in ALC mode when the 'to reg' field contains /7/(111). LS register 1 contains the field length (real number of bytes, to be transferred to the addressed circuit group, reduced by 1).

LS register 6 contains the address of the first CTRL data byte. The field length and the CTRL data address is updated every time a byte is transferred. The field length is decremented by 1, and the CTRL data address is incremented by 1.

The CTRL ALC is used for high speed transfer of a string of bytes (one byte within 2 microseconds) to a single circuit group (eg. print buffer).

Microinstruction Layout

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Op Code				To Reg				SENS/Ctrl Addr							
F				1	1	1	1								

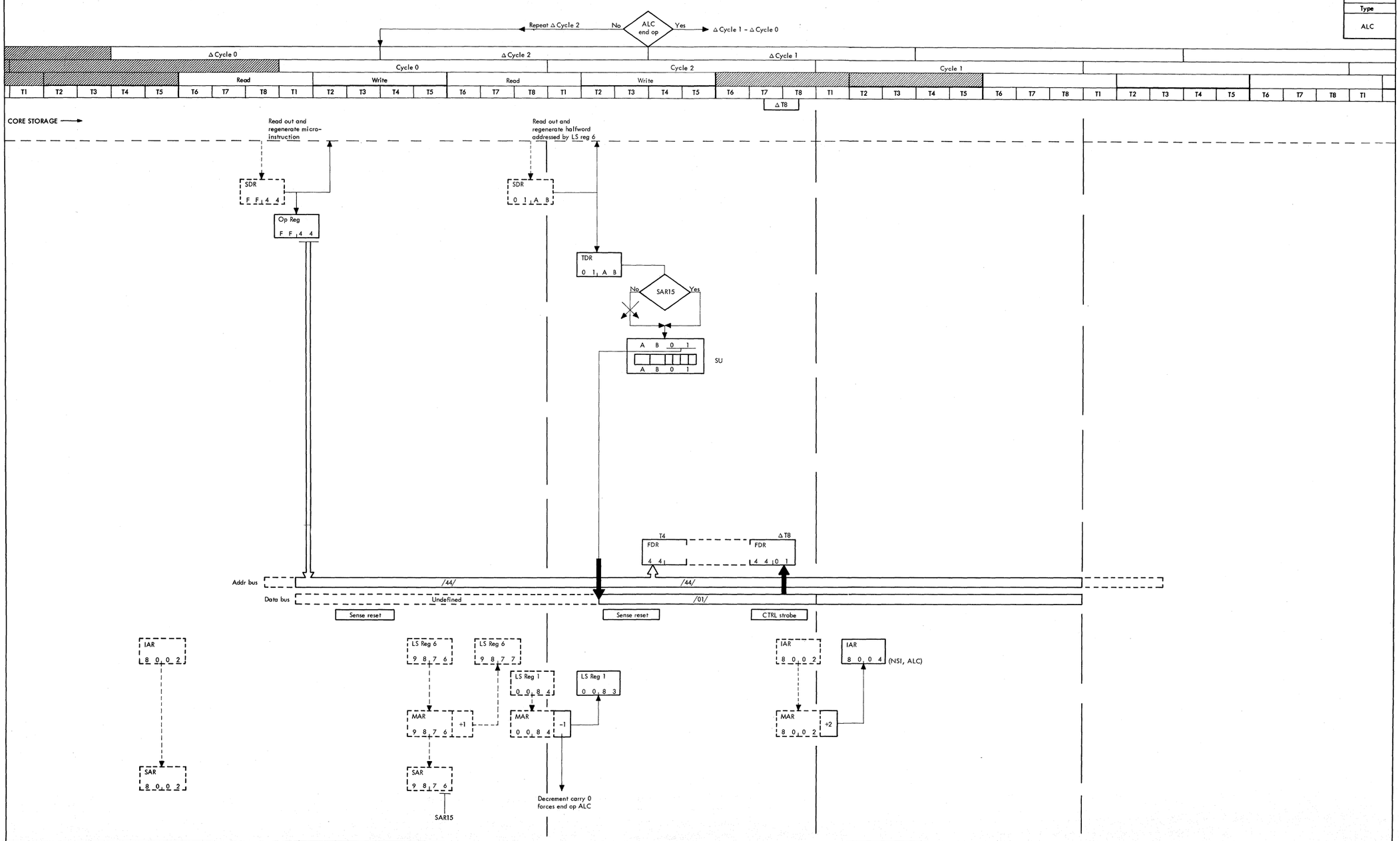
ALC

Mnemonic
CTRL
Format
I/O
Type
ALC

INST	MNEM	OPERANDS	STATEMENTS ACCORDING TO STANDARD CEB 0-1046-XXX
FF44	CTRL	7I, X'44'	CONTROL 44/BY(R6,+1,UNTIL R1,LT,0)

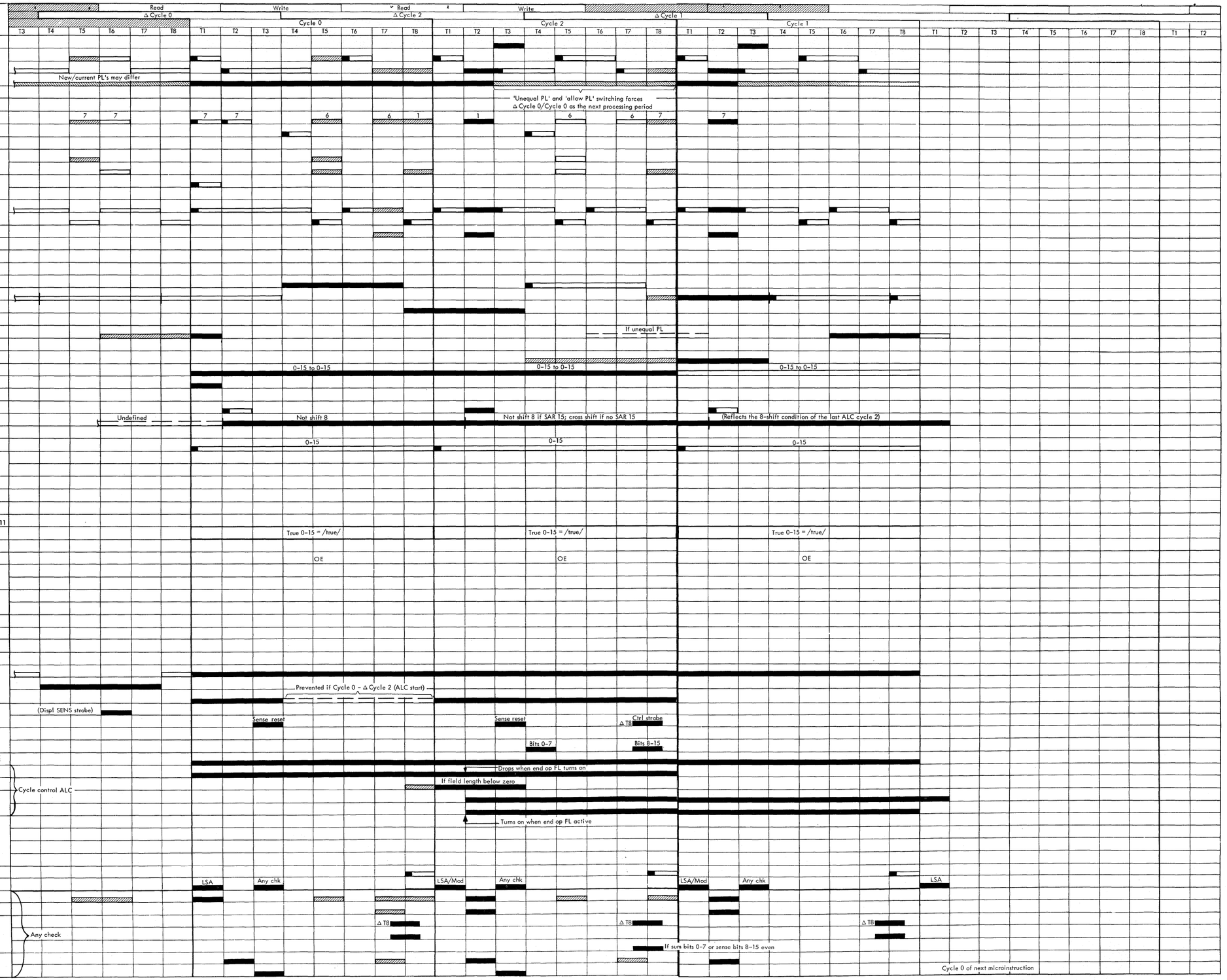
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58	Skip Cy 0 to 2/End Op Cy 1	KA402/403
59	Skip Cycle 2 to 2	KA411
60	Decrement Carry 0	RA301
61	End Op Latch	KA411
62	Skip Cycle 2 to Cycle 1	
63		
64		
65		
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▭

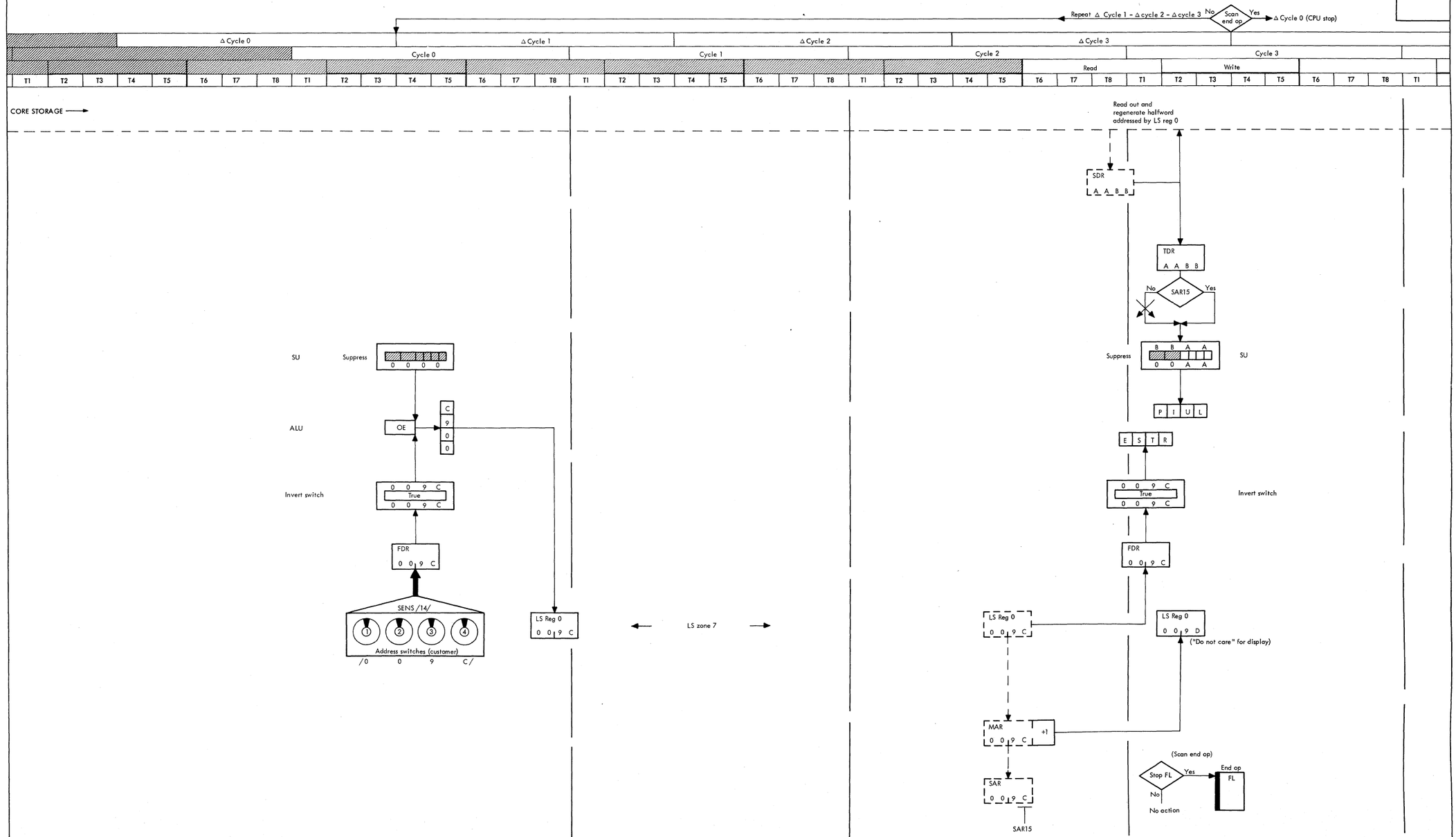
● Diagram 5-72. Control I/O (ALC) (Part 2 of 2) (03777A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

Due to the complexity of the operation and the limited space available on this page, refer to Chapter 6, Field Engineering Theory of Operation, 2020 Processing Unit, System/360 Model 20 (Machines with serial no. 50,000 and above), Form Y33-1021, for description.

Mnemonic
Format
Type

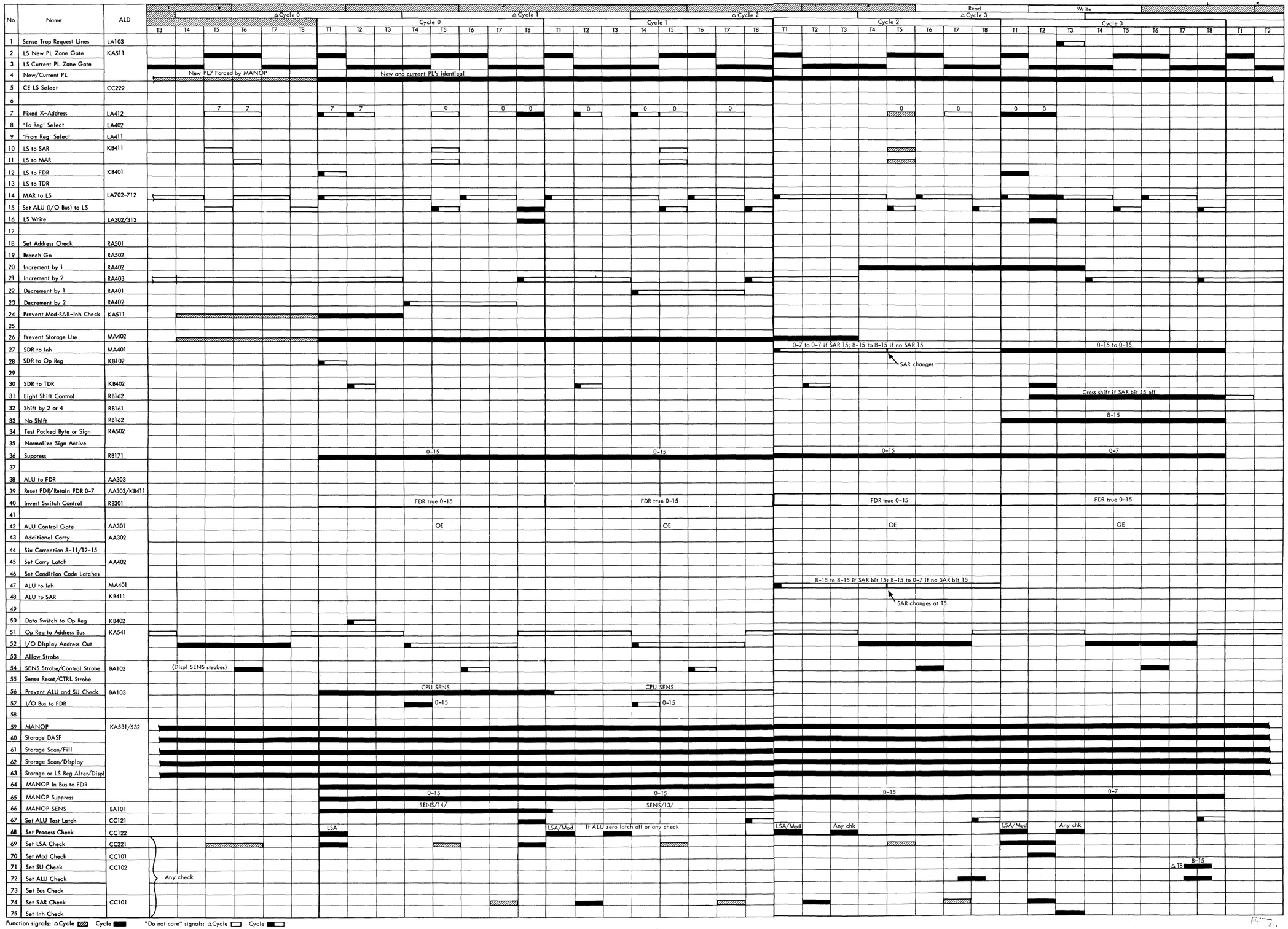
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
- △Cycle
- Cycle



Functions performed during cycle time are shown by full lines and functions performed during △ cycle time are shown by dotted lines.

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59	MANOP	KA531/532
60	Storage DASF	
61	Storage Scan/Fill	
62	Storage Scan/Display	
63	Storage or LS Reg Alter/Displ	
64	MANOP In Bus to FDR	
65	MANOP Suppress	
66	MANOP SENS	BA101
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▬

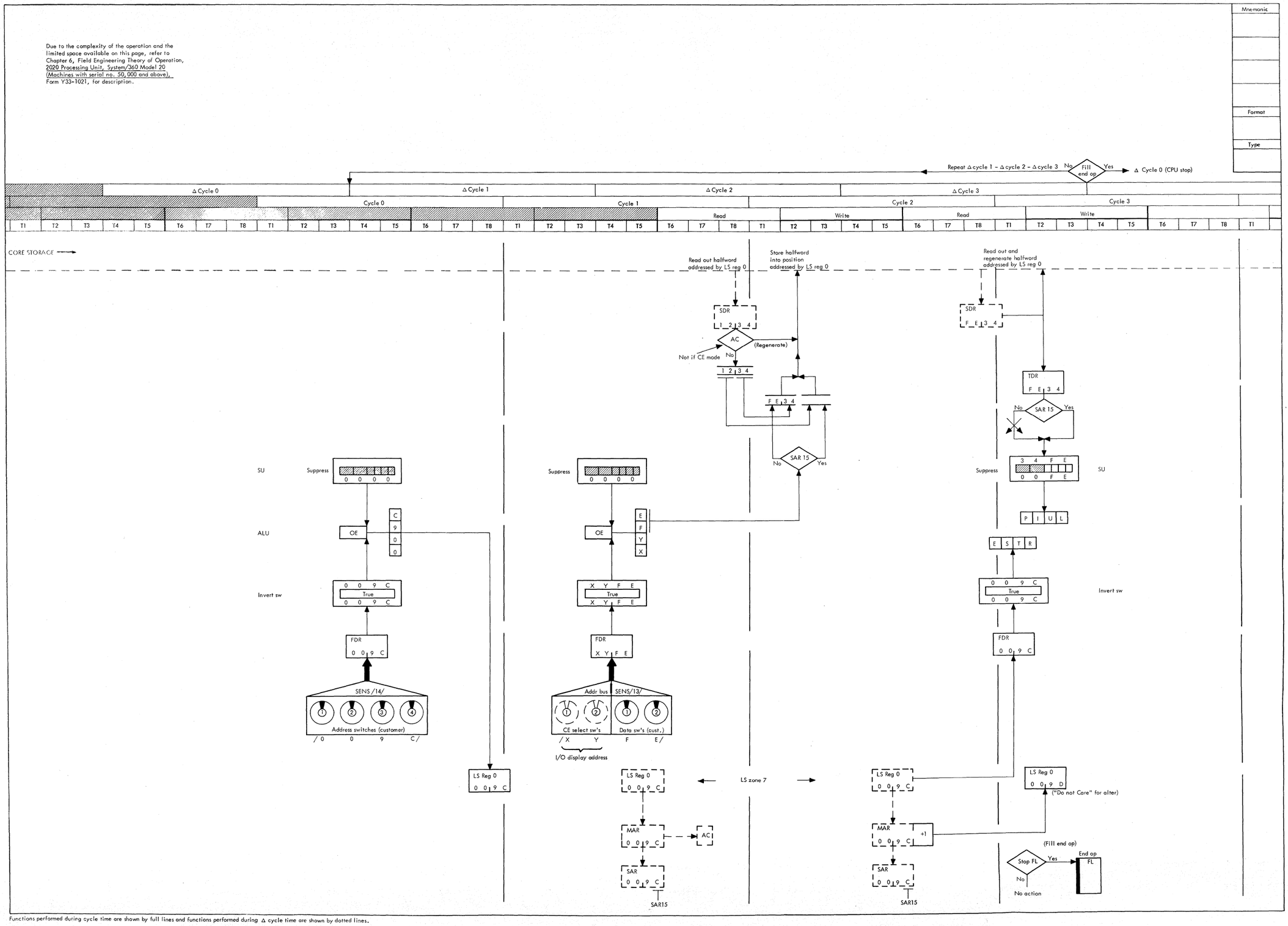
● Diagram 5-73. Storage Display/Scan (Part 2 of 2) (03778A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

Due to the complexity of the operation and the limited space available on this page, refer to Chapter 6, Field Engineering Theory of Operation, 2020 Processing Unit, System/360 Model 20 (Machines with serial no. 50,000 and above), Form Y33-1021, for description.

Mnemonic
Format
Type

Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

Diagram 5-74. Storage Alter/Fill (Part 1 of 2) (03779) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59	MANOP	KA531/532
60	Storage DASF	
61	Storage Scan/Fill	
62	Storage or LS Reg Alter Displ	
63	MANOP In Bus to FDR	
64	MANOP Suppress	
65	MANOP SENS	BA101
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	

Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▭

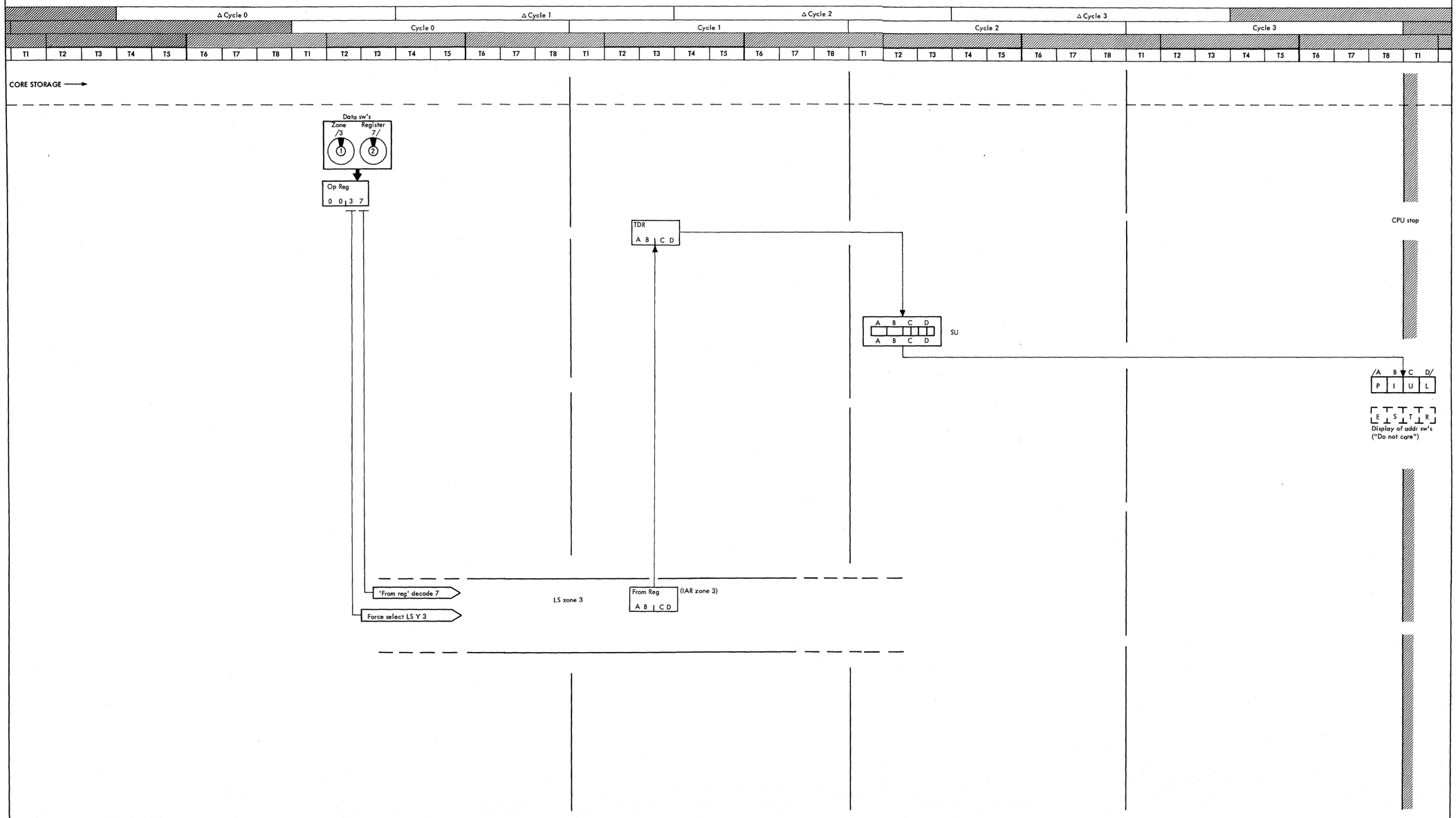
● Diagram 5-74. Storage Alter/Fill (Part 2 of 2) (03779A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

Due to the complexity of the operation and the limited space available on this page, refer to Chapter 6, Field Engineering Theory of Operation, 2020 Processing Unit, System/360 Model 20 (Machines with serial no 50,000 and above), Form Y33-1021, for description.

Mnemonic
Format
Type

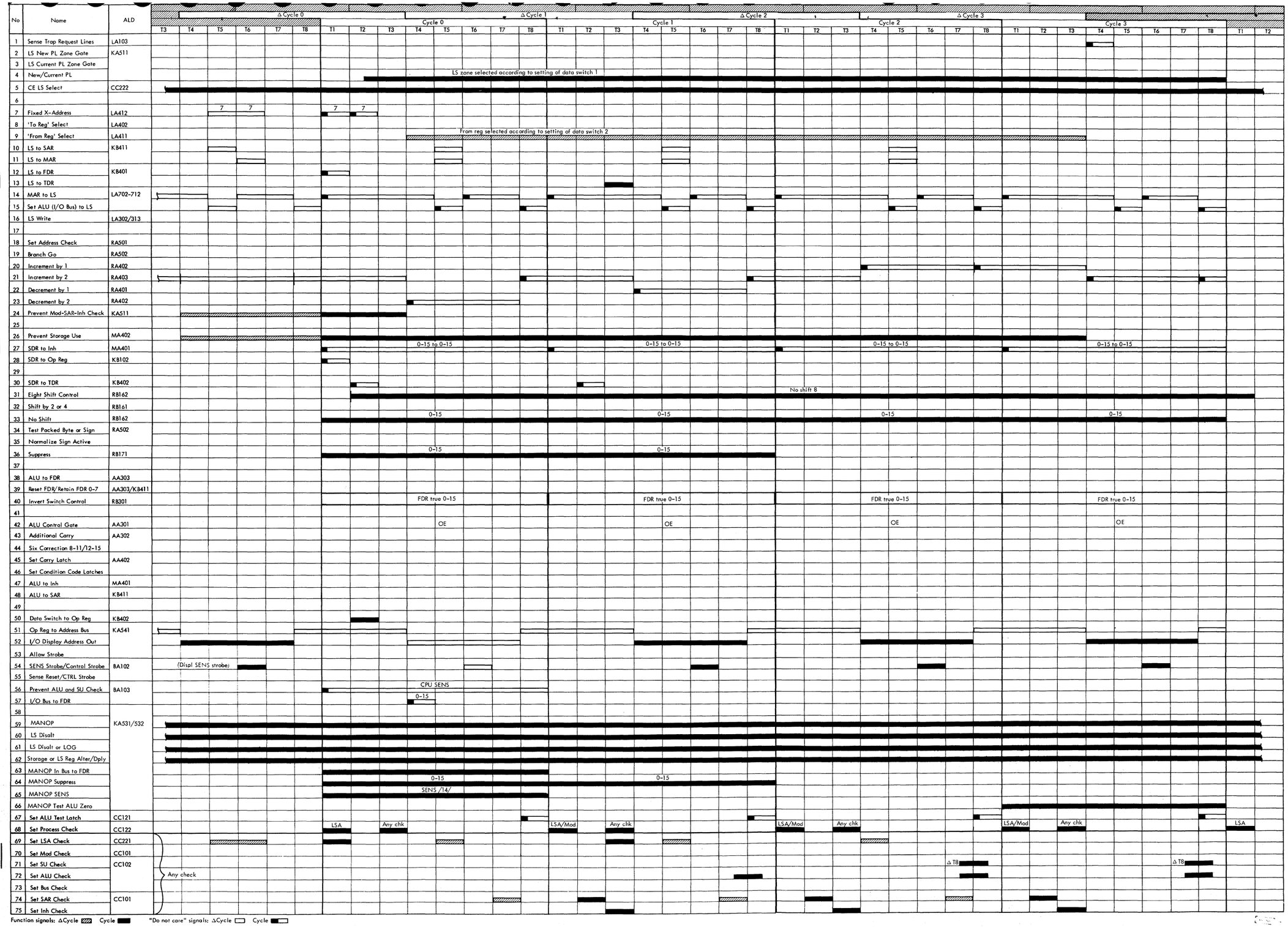
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59	MANOP	KA531/532
60	LS Disalt	
61	LS Disalt or LOG	
62	Storage or LS Reg Alter/Dply	
63	MANOP In Bus to FDR	
64	MANOP Suppress	
65	MANOP SENS	
66	MANOP Test ALU Zero	
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▬

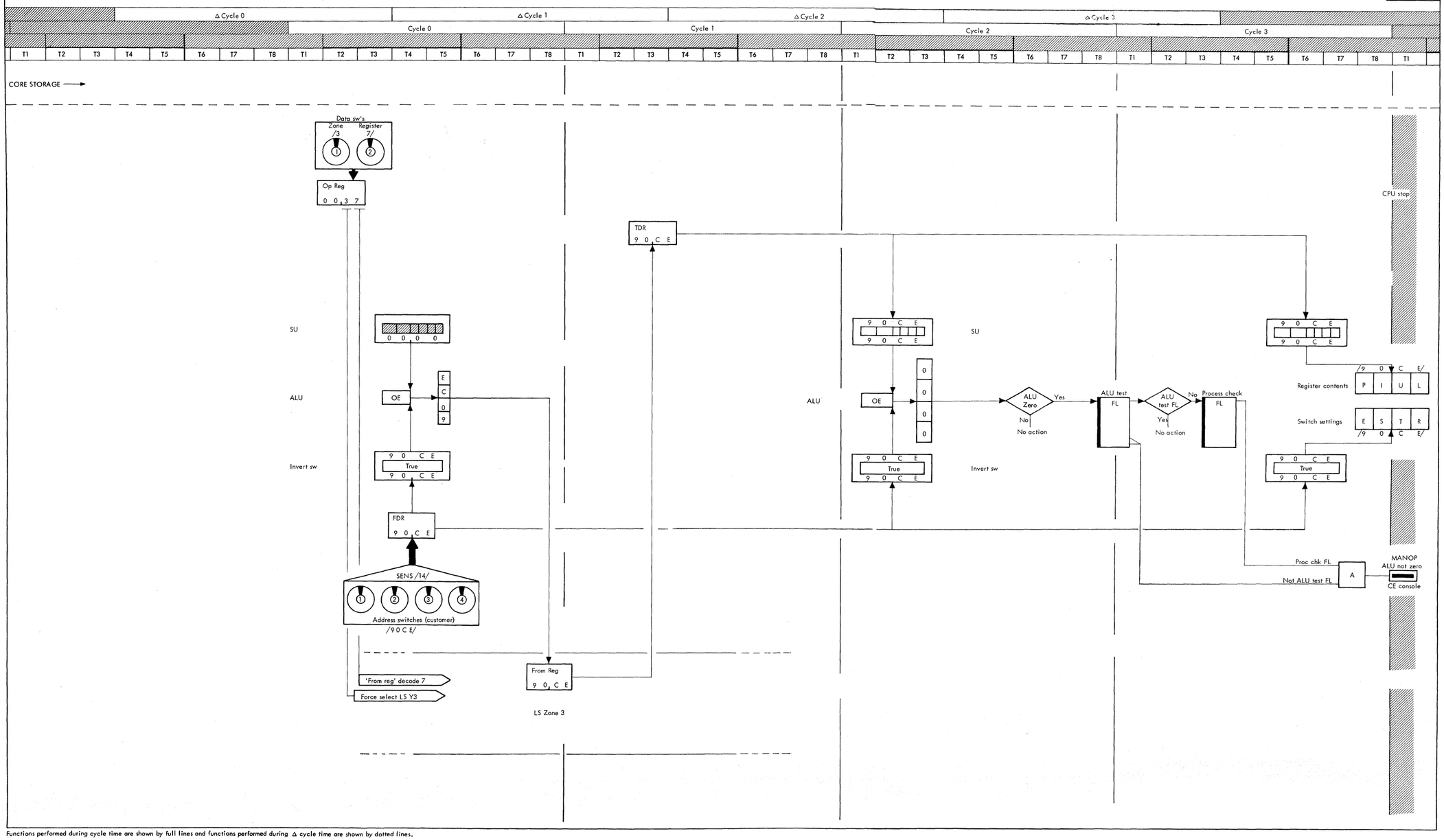
● Diagram 5-75. Local Store Display (Part 2 of 2) (03780A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

Due to the complexity of the operation and the limited space available on this page, refer to Chapter 6, Field Engineering Theory of Operation, 2020 Processing Unit, System/360 Model 20 (Machines with serial no. 50,000 and above), Form Y33-1021, for description.

Mnemonic
Format
Type

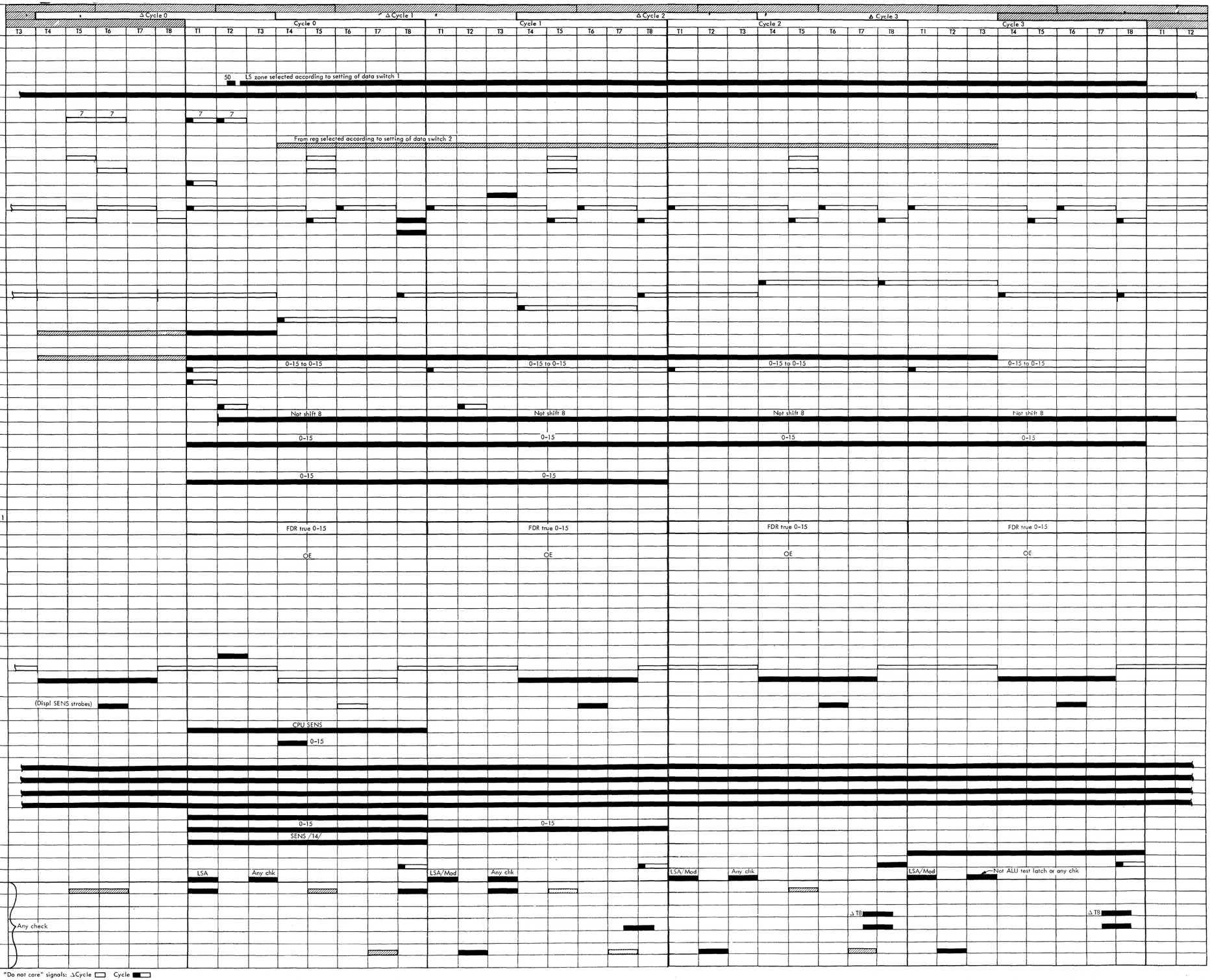
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
- ΔCycle
- Cycle



Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58		
59	MANOP	KA531/532
60	LS Disalter	
61	LS Disalter or LOG	
62	Storage or LS Reg Alter/Displ	
63	MANOP In Bus to FDR	
64	MANOP Suppress	
65	MANOP SENS	
66	MANOP Test ALU Zero	CC122
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▭

● Diagram 5-76. Local Store Alter (Part 2 of 2) (03781A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

Due to the complexity of the operation and the limited space available on this page, refer to Chapter 6, Field Engineering Theory of Operation, 2020 Processing Unit, System/360 Model 20 (Machines with serial no. 50,000 and above), Form Y33-1021, for description.

Mnemonic
Format
Type

Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
- ΔCycle
- Cycle

Repeat ΔCycle 2 - ΔCycle 3 → ICPL end op (No / Yes) → ΔCycle 0

ΔCycle 0 | ΔCycle 1 | ΔCycle 2 | ΔCycle 3

Cycle 0 | Cycle 1 | Cycle 2 | Cycle 3 (Read | Write)

T1 T2 T3 T4 T5 T6 T7 T8 T1 T2 T3 T4 T5 T6 T7 T8 T1 T2 T3 T4 T5 T6 T7 T8 T1 T2 T3 T4 T5 T6 T7 T8 T1

ΔT8 | ΔT8 | ΔT8

CORE STORAGE →

Read out halfword addressed by LS reg 0

Store halfword into position addressed by LS reg 0

Data sw's /2 /0 (1) (2)

Op Reg 0 0 2 0

Note: CPU log in is performed before ICPL (see Diagram 5-80). For ICPL loop the operation stops after cycle 0 when the stop key is operated (stop FL on). To restart ICPL loop press start key.

Any I/O working or stop FL (No → Perform cycle 1 / Yes → Stop and wait)

Trap request 5 (Yes → Perform cycle 2 and cycle 3 / No → Stop and wait)

SDR 0 0 0 0

0 1 0 0

SAR 15 (No / Yes)

Perform cy 2 and cy 3

Trap request 5 (Yes / No → Stop and wait)

Note: No single cycle during ICPL

Suppress 0 0 0 0

OE → 0 0 0 C

C 0 0 0 True C 0 0 0

FDR C 0 0 0

SENS/14/ (1) (2) (3) (4) Address switches (customer)

SU | ALU | Invert sw

Suppress 0 0 0 0

OE → F 4 0 0

0 0 4 F | 0 0 True | 0 1 4 F

FDR 0 1 4 F

SENS/15/ (1) (2) (3) (4) CE select switches

Suppress 0 0 0 0

OE → 1 0 0 0

0 0 0 1 | 0 0 True | 2 0 0 1

FDR 2 0 | FDR 2 0 0 1

Any I/O error (No → Perform cycle 3 / Yes → Check stop)

Addr bus /C000/ /20/ /20/ /20/

Data bus /20/ /05/ /01/

Sense reset | Ctrl strobe | Sense reset | Ctrl strobe | SENS strobe | Control strobe

Force /20/

LS zone 7 →

LS Reg 0 C 0 0 0

LS Reg 0 C 0 0 0

LS Reg 4 0 0 4 F

IAR C 0 0 0

Force /05/ /06/ /46/

CE select sw 1 (0 / 2 / 7)

= 01 11 → Controls the forcing

MAR C 0 0 0 (+0)

LS reg 0 is unchanged and moved into IAR when CPU is started by the first trap-req 5 (cycle 1 overlaps Δ cycle 2)

LS Reg 0 C 0 0 0

LS Reg 0 C 0 0 1

LS Reg 4 0 0 4 F

LS Reg 4 0 0 4 E

MAR C 0 0 0 (+1)

MAR 0 0 4 F (-1)

SAR C 0 0 0

SAR15

Decrement carry 0 forces end op, ICPL

Switch-Settings

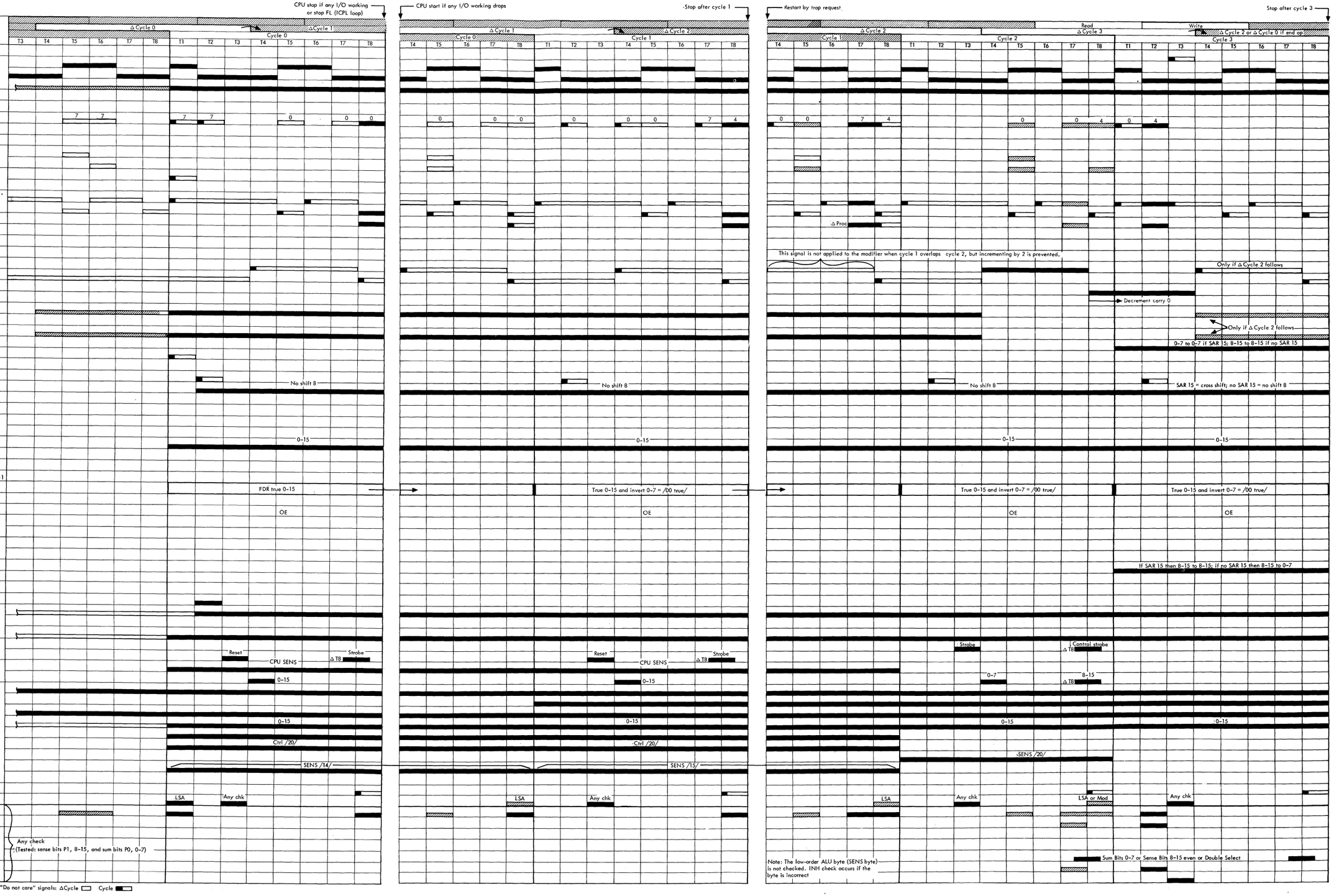
	CE-Sel-Sw's				Data Sw's		Address Sw's			
Load Device	1	2	3	4	1	2	1	2	3	4
2501	0	1								
2520/60-Hopper 1	2	2	> 4	F	2	0	C	0	0	0
2560-Hopper 2	7	2								

Table 1

Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

● Diagram 5-77. Initial Control Program Load (Part 1 of 2) (03782A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58	ICPL Latch	KA531
59	Force Invert 0-7	KA541
60	MANOP	KA531/532
61	MANOP Suppress	
62	MANOP In Bus to FDR	
63	ICPL-CTRL	KA542
64	ICPL-SENS	
65	MANOP SENS	BA101
66		
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



● Diagram 5-77. Initial Control Program Load (Part 2 of 2) (03782A)

Due to the complexity of the operation and the limited space available on this page, refer to Chapter 6, Field Engineering Theory of Operation, 2020 Processing Unit, System/360 Model 20 (Machines with serial no. 50,000 and above), Form Y33-1021, for description.

Mnemonic
Format
Type

Repeat Δ Cycle and cycle-1, 2, 3 — No — Increment carry 0 — Yes → Continue with compare run Δ cycle 0

Δ Cycle 0	Δ Cycle 1	Δ Cycle 2	Δ Cycle 3	Δ Cycle 0 of compare run
Cycle 0	Cycle 1	Cycle 2	Cycle 3	Cycle 0
	Read	Write	Read	Write

T1 T2 T3 T4 T5 T6 T7 T8 T1 T2 T3 T4 T5 T6 T7 T8 T1 T2 T3 T4 T5 T6 T7 T8 T1 T2 T3 T4 T5 T6 T7 T8 T1 T2 T3 T4 T5 T6 T7 T8 T1

CORE STORAGE →

Store true or inverted address into its own position

Read out and regenerate stored address

SDR

TDR

SU — Suppress 0-15 — 0 0 0 0

ALU — OE — 0 0 0 0

Invert sw — Force zeros — 0 0 0 0 / 0 0 0 0

LS Reg 0 — 0 0 0 0

Suppress 0-15 — 0 0 0 0

Run 1

Run 3

OE — 0 F / 0 F / 0 F / 0 F

Parity inverted

Run 1 = true
Run 3 = invert

F F F F / 0 0 0 0 / 0 0 0 0

FDR — 0 0 0 0

LS Reg 0 — 0 0 0 0

LS zone 7

LS Reg 0 — 0 0 0 0

MAR — 0 0 0 0 — +2

Increment carry 0 if /FFFE/+2 (run end)

SAR — 0 0 0 0

LS Reg 0 — 0 0 0 2

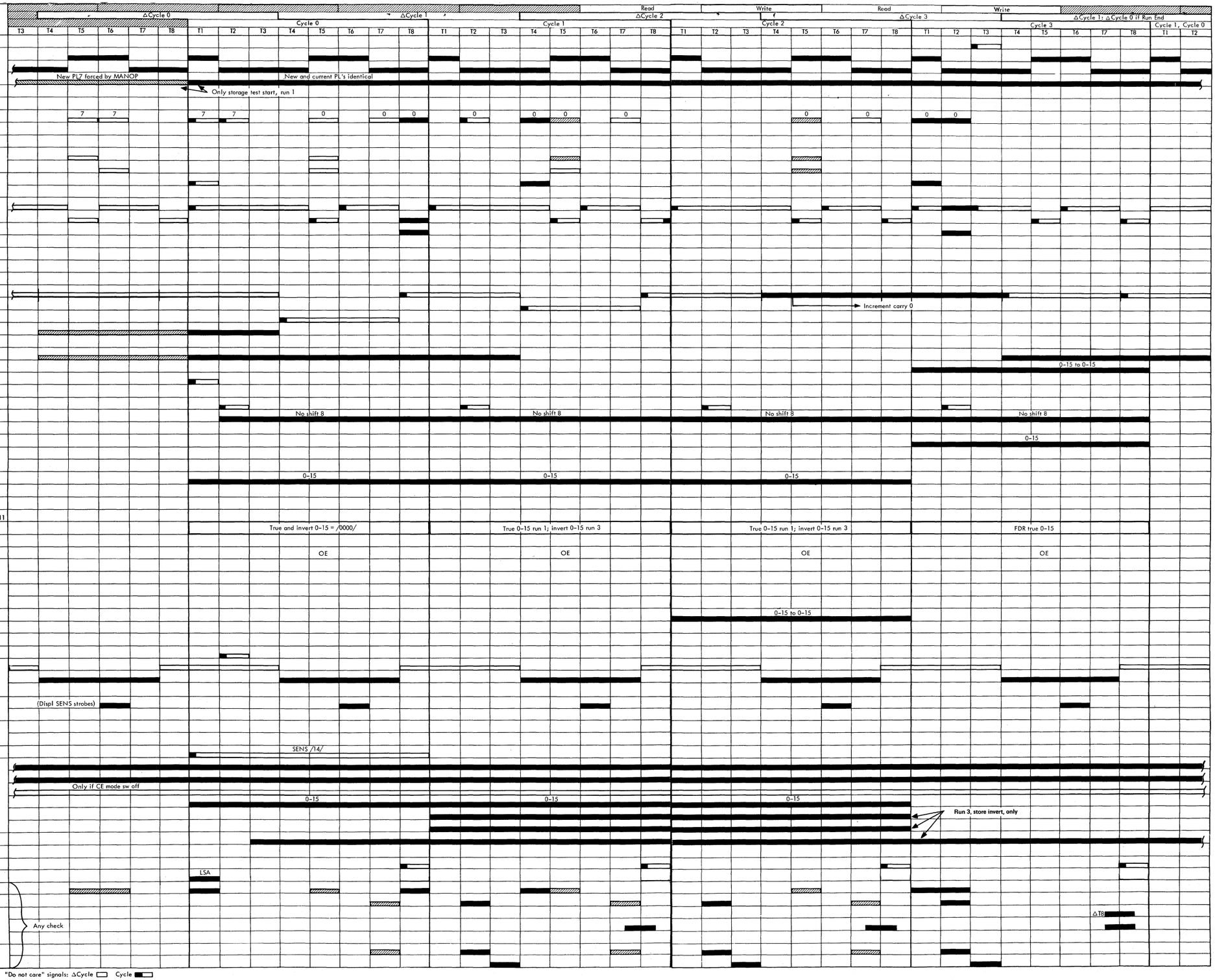
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle

Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

Diagram 5-78. Storage Test Run 1 and 3 (Load Runs) (Part 1 of 2) (03783) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58	Manop SENS	BA101
59	MANOP	KA531/532
60	Storage Test	
61	Storage Fill/Alter not CE Mode	
62	Manop Suppress	
63	Inhibit FDR True 0-15	
64	Manop FDR Invert 0-15	
65	Invert Parity Latch	KA414
66	Manop Test ALU Zero	CC122
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▬

● Diagram 5-78. Storage Test Run 1 and 3 (Load Runs) (Part 2 of 2) (03783A)

Due to the complexity of the operation and the limited space available on this page, refer to Chapter 6, Field Engineering Theory of Operation, 2020 Processing Unit, System/360 Model 20 (Machines with serial no. 50,000 and above), Form Y33-1021, for description.

Mnemonic

Format

Type

Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle

Repeat Δ cycle and cycle -1,2,3 — No — Increment carry 0 — Yes — Continue with load run or CPU stop if run 2 and stop key operated

Δ Cycle 0 | Δ Cycle 1 | Δ Cycle 2 | Δ Cycle 3 | Δ Cycle of next load run

Cycle 0 | Cycle 1 | Cycle 2 | Cycle 3 | Cycle 0

Read | Write | Read | Write

T1 T2 T3 T4 T5 T6 T7 T8 T1 T2 T3 T4 T5 T6 T7 T8 T1 T2 T3 T4 T5 T6 T7 T8 T1 T2 T3 T4 T5 T6 T7 T8 T1

CORE STORAGE →

Read out halfword addressed by LS reg 0

Regen halfword

Read out and read addressed halfword

SDR

Run 2 →
Run 4 →

TDR

Suppress 0-15

OE

Force zeros

SU

ALU

Invert switch

Run 2 = true
Run 4 = invert

ALU test

Storage use

No action

OR

ALU test FL

Process check FL

No action

Display storage halfword in P-I-U-L =/0000/

Display compare address in E-S-T-R

True

Proc chk FL

Not ALU test FL

A

MANOP ALU not zero

Stop if check or stop key op

FDR

LS Reg 0

LS zone 7

SAR

MAR

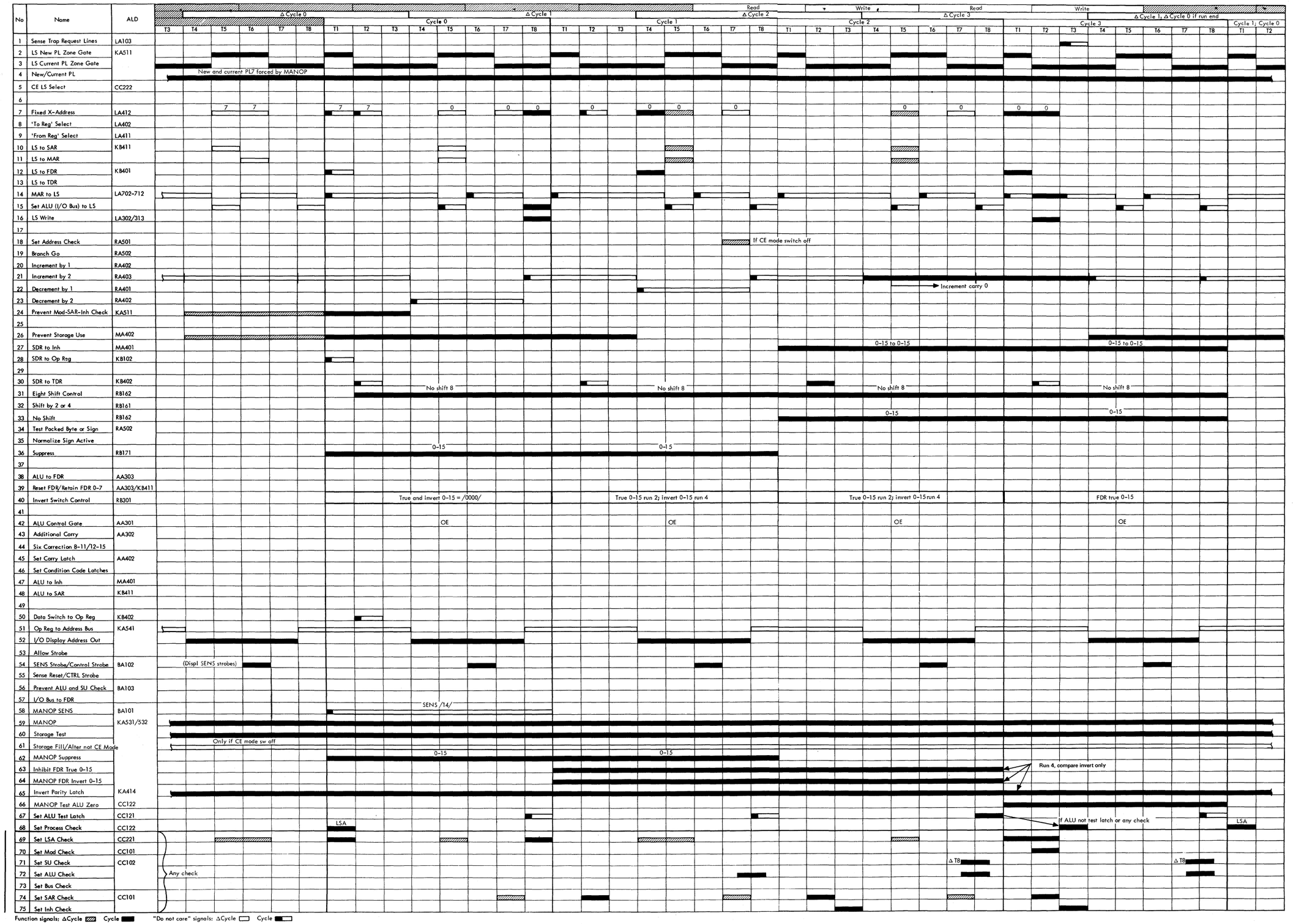
+2

Increment carry 0 if /FFFE/+2 (run end)

Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

Diagram 5-79. Storage Test Run 2 and 4 (Compare Runs) (Part 1 of 2) (03784) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

No	Name	ALD
1	Sense Trap Request Lines	LA103
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
4	New/Current PL	
5	CE LS Select	CC222
6		
7	Fixed X-Address	LA412
8	'To Reg' Select	LA402
9	'From Reg' Select	LA411
10	LS to SAR	KB411
11	LS to MAR	
12	LS to FDR	KB401
13	LS to TDR	
14	MAR to LS	LA702-712
15	Set ALU (I/O Bus) to LS	
16	LS Write	LA302/313
17		
18	Set Address Check	RA501
19	Branch Go	RA502
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
24	Prevent Mod-SAR-Inh Check	KA511
25		
26	Prevent Storage Use	MA402
27	SDR to Inh	MA401
28	SDR to Op Reg	KB102
29		
30	SDR to TDR	KB402
31	Eight Shift Control	RB162
32	Shift by 2 or 4	RB161
33	No Shift	RB162
34	Test Packed Byte or Sign	RA502
35	Normalize Sign Active	
36	Suppress	RB171
37		
38	ALU to FDR	AA303
39	Reset FDR/Retain FDR 0-7	AA303/KB411
40	Invert Switch Control	RB301
41		
42	ALU Control Gate	AA301
43	Additional Carry	AA302
44	Six Correction 8-11/12-15	
45	Set Carry Latch	AA402
46	Set Condition Code Latches	
47	ALU to Inh	MA401
48	ALU to SAR	KB411
49		
50	Data Switch to Op Reg	KB402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
53	Allow Strobe	
54	SENS Strobe/Control Strobe	BA102
55	Sense Reset/CTRL Strobe	
56	Prevent ALU and SU Check	BA103
57	I/O Bus to FDR	
58	MANOP SENS	BA101
59	MANOP	KA531/532
60	Storage Test	
61	Storage Fill/Alter not CE Mode	
62	MANOP Suppress	
63	Inhibit FDR True 0-15	
64	MANOP FDR Invert 0-15	
65	Invert Parity Latch	KA414
66	MANOP Test ALU Zero	CC122
67	Set ALU Test Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▭

● Diagram 5-79. Storage Test Run 2 and 4 (Compare Runs) (Part 2 of 2) (03784A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

Due to the complexity of the operation and the limited space available on this page, refer to Chapter 6, Field Engineering Theory of Operation, 2020 Processing Unit, System/360 Model 20 (Machines with serial no 50,000 and above), Form Y33-1021, for description.

Mnemonic

Format

Type

Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
ΔCycle
Cycle

Any CS Request

Cycle Steal

Δ Cycle 0 | Δ Cycle 1 — retained → Δ Cycle 1 | Δ Cycle 2 | Δ Cycle 3

Cycle 0 | Cycle 1 — retained → Cycle 1 | Cycle 2 | Cycle 3

Read | Write | Read | Write | Read | Write | Read | Write | Read

T1 T2 T3 T4 T5 T6 T7 T8 T1 T2 T3 T4 T5 T6 T7 T8 T1 T2 T3 T4 T5 T6 T7 T8 T1 T2 T3 T4 T5 T6 T7 T8 T1 T2 T3 T4 T5 T6 T7 T8 T1

CS Time T3

CORE STORAGE

Read out and regenerate micro-instruction

SDR C 3 C A (7) (B)

Op Reg C 3 C A (7) (B)

AND OR EOR

An AND (OR, EOR) microinstruction, XX type, is interrupted by a CS operation. The interrupted instruction is shown completely in Diagram 5-49, Part 1.

Read out and regenerate 'from operand'

SDR 1 2 4 8

TDR 1 2 4 8

SAR 15 — No / Yes

Suppress

1 2 4 8 / 0 0 4 8

AND

8 4 0 0

F F F F / F F F F

(1)

IAR 8 0 0 2

MAR 8 0 0 2 +2

IAR 8 0 0 4

ALC — No / Yes — No action

SAR 8 0 0 2

(LS reg 2)

From Reg 0 1 2 3

MAR 0 1 2 3 +1

AC

SAR 0 1 2 3

SAR15

From Reg 0 1 2 4

LS Reg 1 0 0 0 A

LS Reg 1 0 0 0 9

LS Reg 1 0 0 0 A -1

ALC — Yes / No — No action

Decrement carry 0 forces end op ALC

Read out CS halfword

SDR blank

Reset SDR

SDR

CS read=core stor write
CS write=core stor read
Not CS read=CS write
Not CS halfw=CS byte

(Force regen 0-15)

CS read — No / Yes

(Inhibit halfword)

CS halfword — No / Yes

No action

SAR 15 — 0-7 / 8-15

CS halfword — No / Yes — SAR 15 (8-15) / No SAR 15 (0-7)

CS read — No / Yes — No action

CS halfword — No / Yes — SAR 15 / No SAR 15

CS data bus: P0 0-7, P1 8-15

blank / blank

CS data out

CS data in

Store CS halfword

CS inhibit chk

FL

CS read — Yes / No — No action

Parity correct — No / Yes — No action

SDR blank

Reset SDR

FDR blank

Reset FDR

CS LS select

LS zone 1 or 7

Data addr

LS Reg 1 or 3

LS Reg 0 or 2

Field Length

Byte HW +1 +2 Incr

CS incr/decr

Decr Byte HW -1 -2

MAR

CS halfword — No / Yes

-2 — Yes

-1

Outside cust area — Yes / No — No action

CS addr chk

FL

SAR

SAR 15 (CS Byte only)

CS halfw 0 0 0 2 / 0 0 0 1

CS byte

CS counter carry

CS counter zero

Read out and regenerate 'to operand'

SDR A B C D

TDR A B C D

SAR 15 — No / Yes

C D A B / 0 0 A B

/AB/ = 1010 1011

/48/ = 0100 1000

Result:

AND 0000 1000 = /08/

OR 1110 1011 = /EB/

OE 1110 0011 = /E3/

AND-OR-OE

B B 3 / 0 E E / 0 0 0 / 0 0 0

0 0 4 8 / True / 0 0 4 8

FDR 0 0 4 8

To Reg 3 2 1 0 (LS reg 4)

MAR 3 2 1 0 — AC

SAR 3 2 1 0

SAR15

Read out 'to operand'

SDR A B C D

To Reg 3 2 1 0

To Reg 3 2 1 1

IAR 8 0 0 2

MAR 3 2 1 0 +1

MAR 8 0 0 2 +2

SAR 3 2 1 0 — AC

SAR15

For continuation of instruction see Diagram 5-49, Part 1

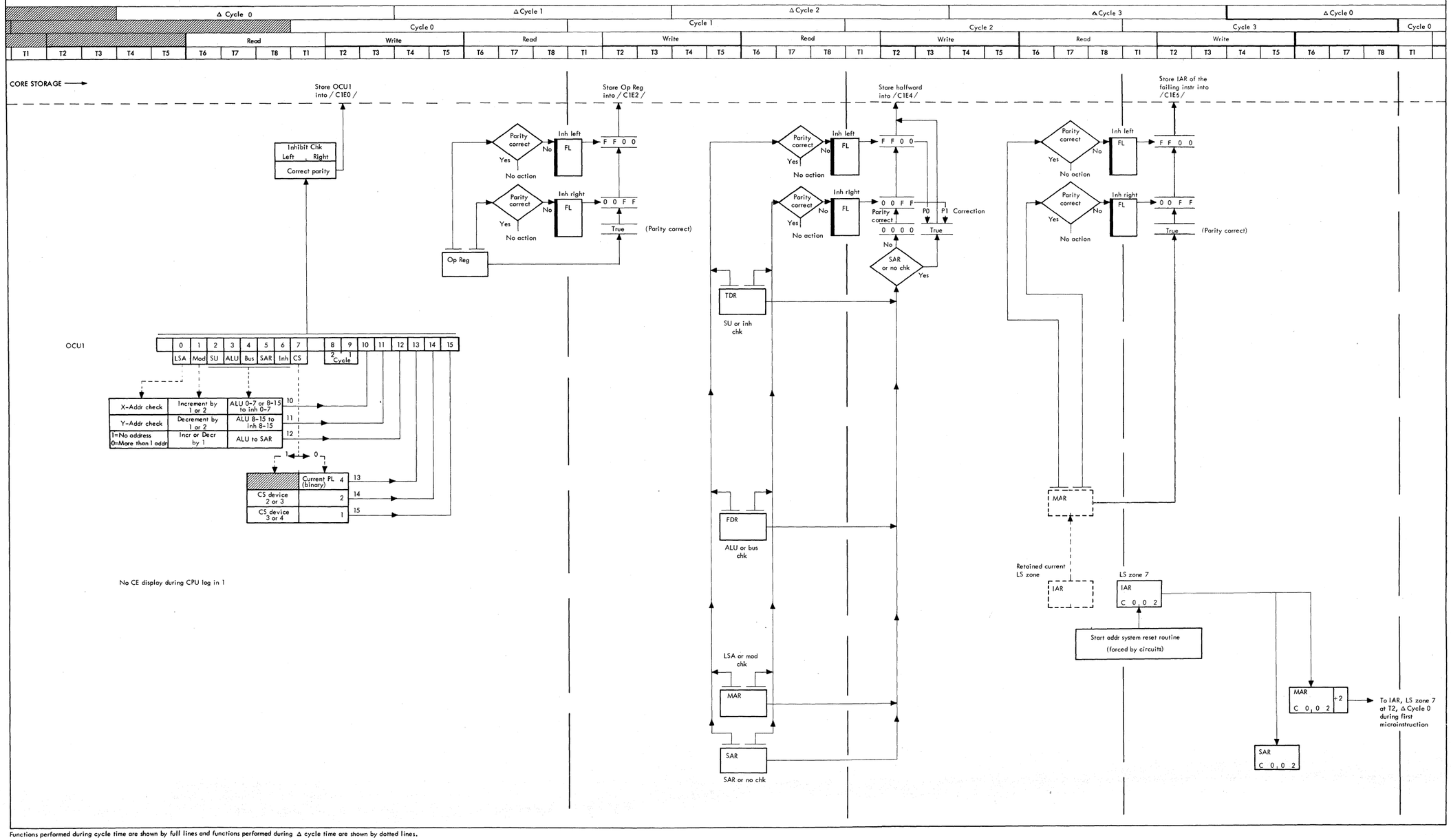
Functions performed during cycle time are shown by full lines and functions performed during Δ cycle time are shown by dotted lines.

Due to the complexity of the operation and the limited space available on this page, refer to Chapter 6, Field Engineering Theory of Operation, 2020 Processing Unit, System/360 Model 20 (Machines with serial no. 50,000 and above), Form Y33-1021, for description.

Mnemonic
Format
Type

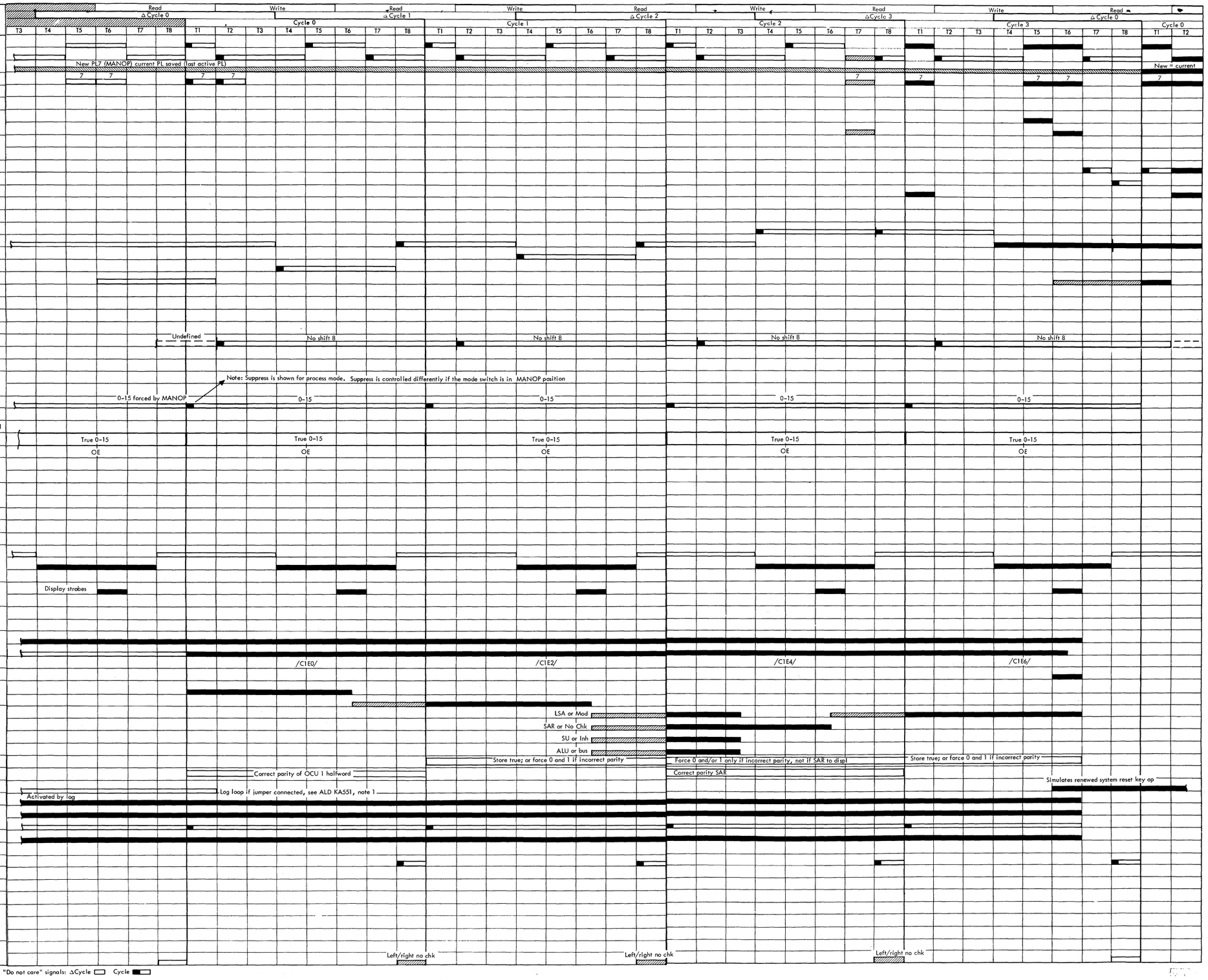
Note: For "Do not care" functions refer to timing chart below.

"Do not care" signals:
- △Cycle
- Cycle



Functions performed during cycle time are shown by full lines and functions performed during △ cycle time are shown by dotted lines.

No	Name	ALD
1	LS New PL Zone Gate	KA511
2	LS Current PL Zone Gate	
3	New/Current PL	
4	Fixed X-Address	LA412
5	'To Reg' Select	LA402
6	'From Reg' Select	LA411
7	LS to SAR	KB411
8	LS to MAR	
9	LS to FDR	KB401
10	LS to TDR	
11	MAR to LS	LA702
12	ALU (I/O Bus) to LS	KB412
13	LS Write	LA302/313
14	Set Address Check	RA501
15	Branch Go	RA502
16	Increment by 1	RA402
17	Increment by 2	RA403
18	Decrement by 1	RA401
19	Decrement by 2	RA402
20	Prevent Modifier Check	KA511
21	Prevent Storage Use	MA402
22	SDR to Inh	MA401
23	SDR to Op Reg	KB102
24	SDR to TDR	KB402
25	Eight Shift Control	RB162
26	Shift by 2 or 4	RB161
27	No Shift	RB162
28	Test Packed Byte or Sign	RA502
29	Normalize Sign Active	
30	Suppress	RB171
31	ALU to FDR	AA303
32	Reset FDR/Retain FDR 0-7	AA303/KB411
33	Invert Switch Control	RB301
34	ALU Control Gate	AA301
35	Additional Carry	AA302
36	Six Correction 8-11/12-15	
37	Set Carry Latch	AA402
38	Set Condition Code Latches	
39	ALU to Inh	MA401
40	ALU to SAR	KB411
41	Data Switch to Op Reg	KB402
42	Op Reg to Address Bus	KA541
43	I/O Display Address Out	
44	Allow Strobe	
45	SENS Strobe/Control Strobe	BA102
46	Sense Reset/CTRL Strobe	
47	Prevent ALU and SU Check	BA103
48	I/O Bus to FDR	
49	Log Latch	KA551
50	Log SAR Power	
51	Log Addresses	MA211/221
52	Log Reset	KA551
53	OCU 1 to Display	KA552
54	Op Reg to Display	
55	MAR to Display	KA553
56	SAR to Display	
57	TDR to Display	
58	FDR to Display	
59	Force Zeros or Ones	KA552
60	Correct Parity OCU 1, SAR	BA221
61	Log Force System Reset	KA551
62	MANOP	KA531
63	LS Disalter or Log	KA532
64	MANOP Suppress	
65	Force Address /C002/	LA701
66		
67	Set ALU Zero Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	



Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▬

Diagram 5-80. CPU LOG IN (Part 2 of 2) (03785A) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

No	Name	ALD
	Sense CS Request	CS102
	CS Request Latch (1,2,3or4)	CS201-31
	Any CS Request	CS101
	Cycle Steal (latch)	
	CS Control Signals Gated	CS201-31
	CS Read Latch	CS112
	CS Halfword Latch	
	CS Select (1, 2, 3 or 4)	CS201-31
	CS Device Latches (1,2,3or4)	CS101
2	LS New PL Zone Gate	KA511
3	LS Current PL Zone Gate	
	CS LS Select Time	
7	Fixed X-Address	LA412
10	LS to SAR	KB411
11	LS to MAR	
14	MAR to LS	LA702
15	ALU (I/O Bus) to LS	KB412
16	LS Write	LA302/313
	Set CS Address Check	CS112
20	Increment by 1	RA402
21	Increment by 2	RA403
22	Decrement by 1	RA401
23	Decrement by 2	RA402
51	Op Reg to Address Bus	KA541
52	I/O Display Address Out	
	Display SENS Strobe	BA102
67	Set ALU Zero Latch	CC121
68	Set Process Check	CC122
69	Set LSA Check	CC221
70	Set Mod Check	CC101
71	Set SU Check	CC102
72	Set ALU Check	
73	Set Bus Check	
74	Set SAR Check	CC101
75	Set Inh Check	
	Addressed Halfword in SDR	
	CS Data Out Gate	CS111
	Force Regen SDR	CS501
	CS Store	CS501
	Force Regen SDR	CS501
	Set CS inhibit check	CS111
	Set CS interface check	

Read, Write, Read, Write, Read, Write, Read — ΔCycle 0, Cycle 0, ΔCycle 1, Cycle 1, ΔCycle 2, Cycle 2, ΔCycle 3, Cycle 3; T1 T2 T3 T4 T5 T6 T7 T8

Reset during next CS request

R 0 or 2 | W 0 or 2 | R 1 or 3 | W 1 or 3

Controlled by CS incr/decr and CS byte/halfword

Controlled by CS byte/halfword

Control is different for SENS, ctrl

LSA/Mod

Any chk

Any check

Only if no CS read (CS write)

0-15 if CS halfword; if CS byte 0-7 if no SAR 15 – 8-15 if SAR 15

Note: The out gates remain according to the last requested CS format. CS byte gating is controlled by SAR 15. Thus, the gate changing is undefined.

0-15 if CS write

0-15 if CS halfword; if CS byte = 0-7 if no SAR 15, 8-15 if SAR 15

(Only if CS byte) 0-7 if SAR 15, 8-15 if no SAR 15

CS checks do not cause process check

CS read only

Interface or address check resets CS read

Any CS request

Cycle steal (CS)

Function signals: ΔCycle ▨ Cycle ■ "Do not care" signals: ΔCycle □ Cycle ▬

Diagram 5-81. CPU Cycle Steal Operation (Part 2 of 2) (03786) 2020 ≥ 50,000 FEMDM Vol 2 (8/69)

READER'S COMMENT FORM

2020 Processing Unit, System/360 Model 20 (Machines with serial no. 50,000 and above), Volume 2 FEMDM

Form SY33-1042-1

How did you use this publication?

As a reference source ☐

As a class-room text ☐

As a self-study text ☐

Based on your own experience, rate this publication:

As a reference source—Very Good ☐ Good ☐ Fair ☐ Poor ☐ Very Poor ☐

As a text—Very Good ☐ Good ☐ Fair ☐ Poor ☐ Very Poor ☐

What is your occupation?

We would appreciate your specific comments; please give page and line references where appropriate. If you wish a reply, be sure to include your name and address.

● Thank you for your cooperation. No postage necessary if mailed in U.S.A.

READER'S COMMENT FORM

2020 Processing Unit, System/360 Model 20 (Machines with serial no. 50,000 and above), Volume 2 FEMDM

Form SY33-1042-1

How did you use this publication?

As a reference source ☐

As a class-room text ☐

As a self-study text ☐

Based on your own experience, rate this publication:

As a reference source—Very Good ☐ Good ☐ Fair ☐ Poor ☐ Very Poor ☐

As a text—Very Good ☐ Good ☐ Fair ☐ Poor ☐ Very Poor ☐

What is your occupation?

We would appreciate your specific comments; please give page and line references where appropriate. If you wish a reply, be sure to include your name and address.

● Thank you for your cooperation. No postage necessary if mailed in U.S.A.

YOUR COMMENTS, PLEASE . . .

This Field Engineering manual is part of a library that serves as a reference source for customer engineers. Your answers to the questions on the back of this form, together with your comments, will help us produce better publications for your use. Each reply will be carefully reviewed by the persons responsible for writing and publishing this material. All comments and suggestions become the property of IBM.

Please note: Requests for copies of publications and for assistance in utilizing your IBM system should be directed to your IBM representative or to the IBM sales office serving your locality.

Fold Fold

FIRST CLASS
PERMIT NO. 1359
WHITE PLAINS, N.Y.

BUSINESS REPLY MAIL

NO POSTAGE STAMP NECESSARY IF MAILED IN THE UNITED STATES

POSTAGE WILL BE PAID BY...

IBM CORPORATION

112 EAST POST ROAD,

WHITE PLAINS, N.Y. 10601.

Attention: Department 813 (B)

Fold Fold

IBM

International Business Machines Corporation
Field Engineering Division
112 East Post Road, White Plains, N.Y. 10601

Cut along this line

SY33-1042-1

YOUR COMMENTS, PLEASE . . .

This Field Engineering manual is part of a library that serves as a reference source for customer engineers. Your answers to the questions on the back of this form, together with your comments, will help us produce better publications for your use. Each reply will be carefully reviewed by the persons responsible for writing and publishing this material. All comments and suggestions become the property of IBM.

Please note: Requests for copies of publications and for assistance in utilizing your IBM system should be directed to your IBM representative or to the IBM sales office serving your locality.

Fold Fold

FIRST CLASS
PERMIT NO. 1359
WHITE PLAINS, N.Y.

BUSINESS REPLY MAIL

NO POSTAGE STAMP NECESSARY IF MAILED IN THE UNITED STATES

POSTAGE WILL BE PAID BY...

IBM CORPORATION

112 EAST POST ROAD,

WHITE PLAINS, N.Y. 10601.

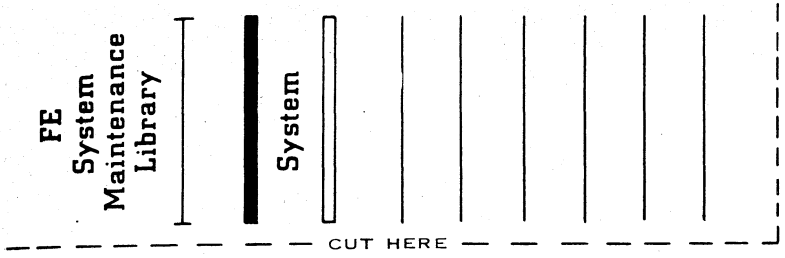
Attention: Department 813 (B)

Fold Fold

IBM

International Business Machines Corporation
Field Engineering Division
112 East Post Road, White Plains, N.Y. 10601

Cut along this line



SY33-1042-1

IBM®
International Business Machines Corporation
Field Engineering Division
112 East Post Road, White Plains, N.Y. 10601

Printed in U.S.A. SY33-1042-1