



# PSMN1R0-40YLD

N-channel 40 V, 1.1 mΩ, 280 A logic level MOSFET in LFPAK56 using NextPower-S3 Schottky-Plus technology

30 November 2017

Product data sheet

## 1. General description

280 Amp, logic level gate drive N-channel enhancement mode MOSFET in 150 °C LFPAK56 package using advanced TrenchMOS Superjunction technology. This product has been designed and qualified for high performance power switching applications.

## 2. Features and benefits

- 280 A capability
- Avalanche rated, 100% tested at  $I_{AS} = 190$  A
- NextPower-S3 technology delivers 'superfast switching with soft recovery'
- Low  $Q_{RR}$ ,  $Q_G$  and  $Q_{GD}$  for high system efficiency and low EMI designs
- Schottky-Plus body-diode, gives soft switching without the associated high  $I_{DSS}$  leakage
- Optimised for 4.5 V gate drive utilising NextPower-S3 Superjunction technology
- High reliability LFPAK (Power SO8) package, copper-clip, solder die attach and qualified to 150 °C
- Exposed leads can be wave soldered, visual solder joint inspection and high quality solder joints
- Low parasitic inductance and resistance

## 3. Applications

- Synchronous rectification
- DC-to-DC converters
- High performance & high efficiency server power supply
- Motor control
- Power ORing

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	-	40	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>	[1]	-	280	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>	-	-	198	W
$T_j$	junction temperature		-55	-	150	°C
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 10</a> ; <a href="#">Fig. 11</a>	-	1.1	1.4	mΩ
		$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 10</a> ; <a href="#">Fig. 11</a>	-	0.93	1.1	mΩ

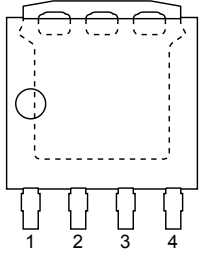
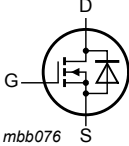
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$I_D = 25\text{ A}$ ; $V_{DS} = 20\text{ V}$ ; $V_{GS} = 4.5\text{ V}$ ; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	-	17	-	nC
$Q_{G(\text{tot})}$	total gate charge		-	59	-	nC

[1] 280A continuous current has been successfully demonstrated during application tests. Practically, the current will be limited by PCB, thermal design and operation temperature.

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p><b>LPAK56; Power-SO8 (SOT1023)</b></p>	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN1R0-40YLD	LPAK56; Power-SO8	Plastic single-ended surface-mounted package (LPAK56); 4 leads	SOT1023

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN1R0-40YLD	1D040L

## 8. Limiting values

**Table 5. Limiting values**

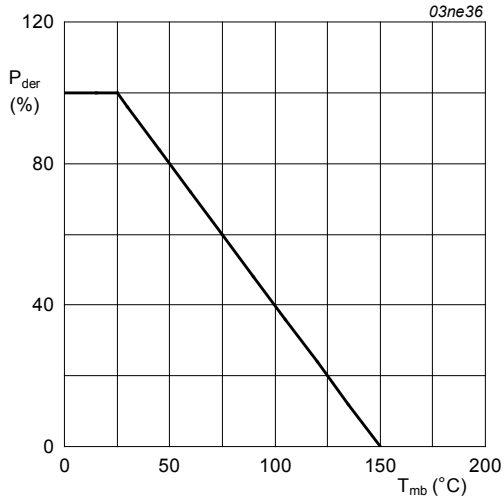
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 150 °C		-	40	V
V <sub>DSM</sub>	peak drain-source voltage	t <sub>p</sub> ≤ 20 ns; f ≤ 500 kHz; E <sub>DS(AL)</sub> ≤ 200 nJ; pulsed		-	45	V
V <sub>DGR</sub>	drain-gate voltage	25 °C ≤ T <sub>j</sub> ≤ 150 °C; R <sub>GS</sub> = 20 k $\Omega$		-	40	V
V <sub>GS</sub>	gate-source voltage			-20	20	V
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <a href="#">Fig. 1</a>		-	198	W
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; <a href="#">Fig. 2</a>	<a href="#">[1]</a>	-	280	A
		V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 100 °C; <a href="#">Fig. 2</a>		-	198	A
I <sub>DM</sub>	peak drain current	pulsed; t <sub>p</sub> ≤ 10 $\mu$ s; T <sub>mb</sub> = 25 °C; <a href="#">Fig. 3</a>		-	1284	A
T <sub>stg</sub>	storage temperature			-55	150	°C
T <sub>j</sub>	junction temperature			-55	150	°C
T <sub>slid(M)</sub>	peak soldering temperature			-	260	°C
V <sub>ESD</sub>	electrostatic discharge voltage	HBM		2	-	kV
<b>Source-drain diode</b>						
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C		-	165	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 $\mu$ s; T <sub>mb</sub> = 25 °C		-	1284	A
<b>Avalanche ruggedness</b>						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	I <sub>D</sub> = 85 A; V <sub>sup</sub> ≤ 40 V; R <sub>GS</sub> = 50 $\Omega$ ; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; unclamped; t <sub>p</sub> = 0.26 ms	<a href="#">[2]</a>	-	578	mJ
		I <sub>D</sub> = 25 A; V <sub>sup</sub> ≤ 40 V; R <sub>GS</sub> = 50 $\Omega$ ; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; unclamped; t <sub>p</sub> = 3.8 ms	<a href="#">[2]</a>	-	2472	mJ
I <sub>AS</sub>	non-repetitive avalanche current	V <sub>sup</sub> ≤ 40 V; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; R <sub>GS</sub> = 50 $\Omega$	<a href="#">[2]</a>	-	190	A

[1] 280A continuous current has been successfully demonstrated during application tests. Practically, the current will be limited by PCB, thermal design and operation temperature.

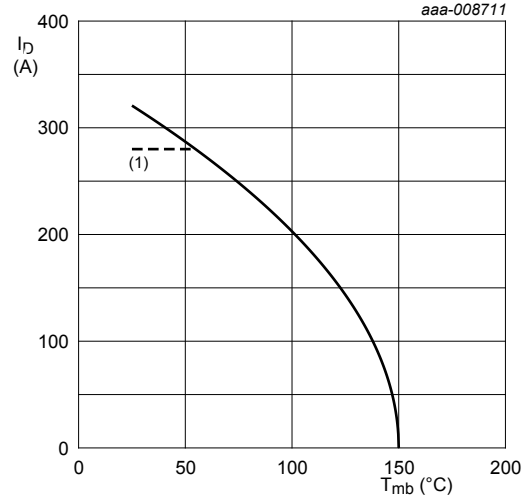
[2] Protected by 100% test

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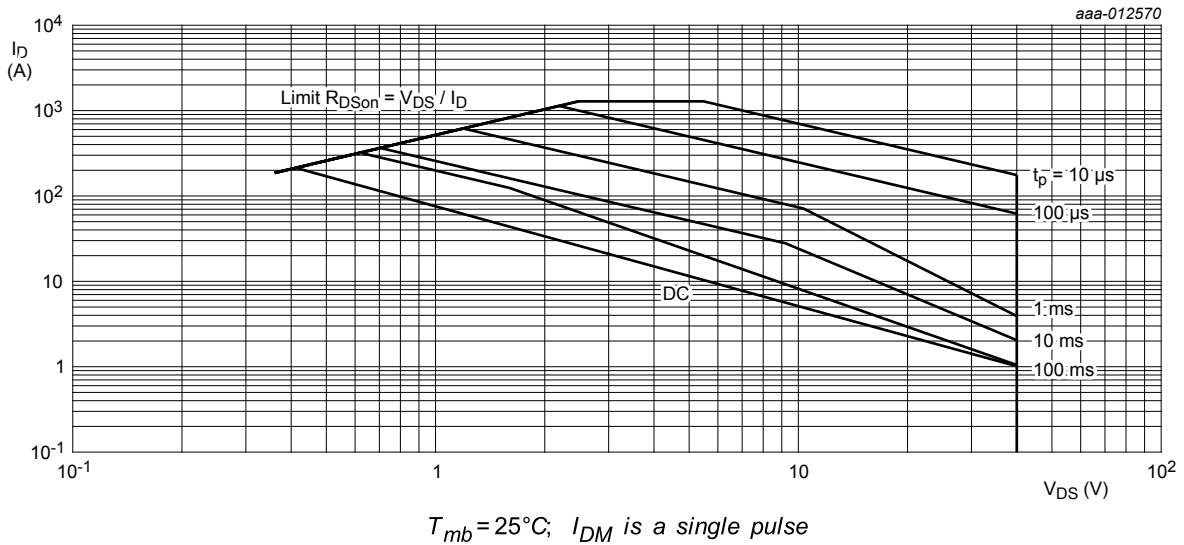
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100\%$$

**Fig. 1. Normalized total power dissipation as a function of mounting base temperature**



(1) 280A continuous current has been successfully demonstrated during applications tests. Practically, the current will be limited by PCB, thermal design and operating temperature.  
 $V_{GS} \geq 10V$

**Fig. 2. Continuous drain current as a function of mounting base temperature**



**Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

### 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Fig. 4</a>	-	0.56	0.63	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	<a href="#">Fig. 5</a>	-	50	-	K/W
		<a href="#">Fig. 6</a>	-	125	-	K/W

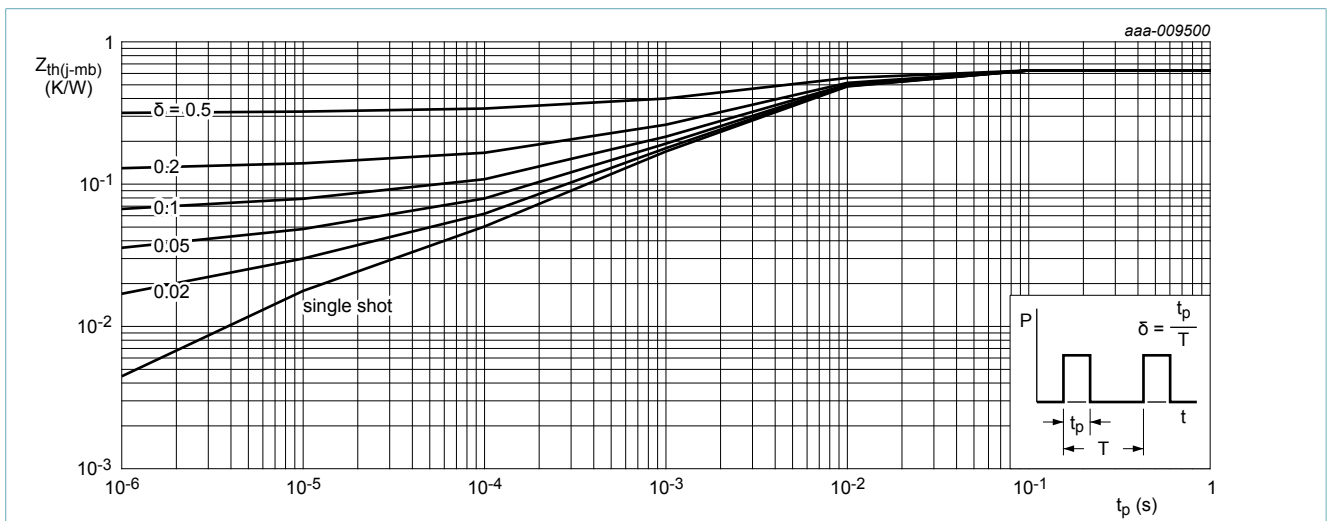


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

aaa-005750

aaa-005751

**Fig. 5.** PCB layout for thermal resistance junction to ambient 1" square pad; FR4 Board; 2oz copper

**Fig. 6.** PCB layout for thermal resistance junction to ambient minimum footprint; FR4 Board; 2oz copper

## 10. Characteristics

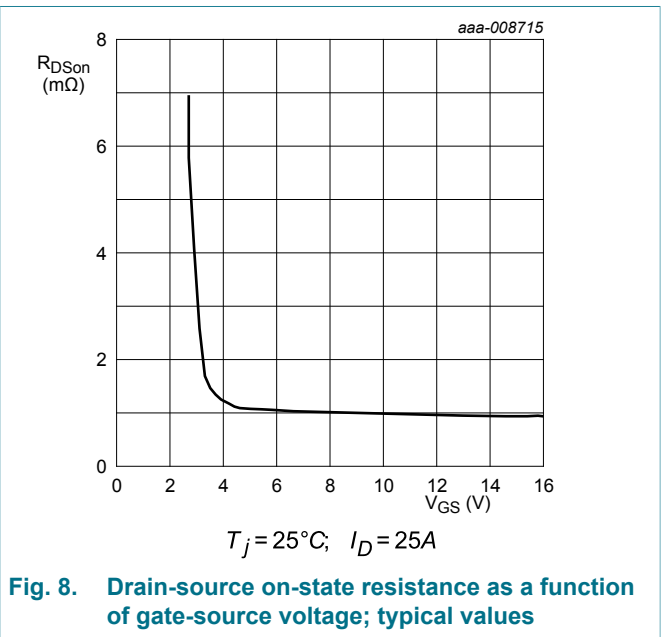
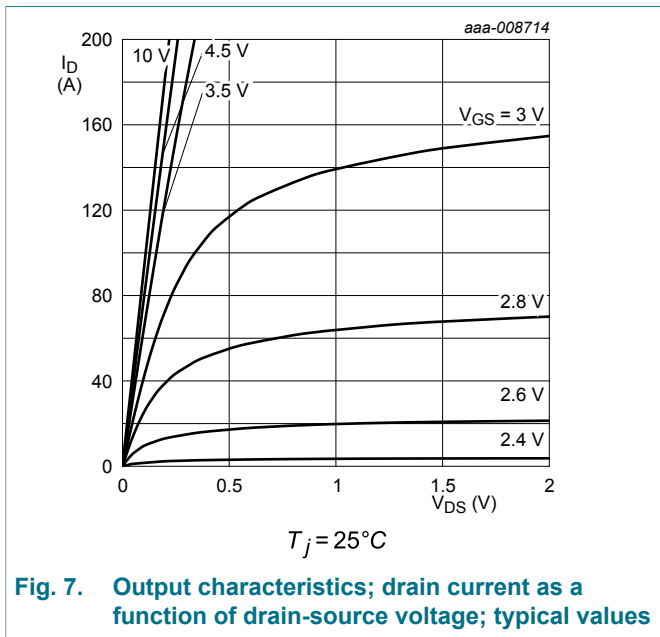
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	40	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$	1.05	1.7	2.2	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 \text{ }^\circ C \leq T_j \leq 150 \text{ }^\circ C$	-	-5.1	-	mV/K
$I_{DSS}$	drain leakage current	$V_{DS} = 32 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	1	$\mu A$
		$V_{DS} = 32 V; V_{GS} = 0 V; T_j = 125 \text{ }^\circ C$	-	9	-	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	100	nA
		$V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 25 A; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 10; Fig. 11</a>	-	0.93	1.1	mΩ
		$V_{GS} = 10 V; I_D = 25 A; T_j = 150 \text{ }^\circ C;$ <a href="#">Fig. 10; Fig. 11</a>	-	-	1.93	mΩ
		$V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 10; Fig. 11</a>	-	1.1	1.4	mΩ
		$V_{GS} = 4.5 V; I_D = 25 A; T_j = 150 \text{ }^\circ C;$ <a href="#">Fig. 10; Fig. 11</a>	-	-	2.45	mΩ
$R_G$	gate resistance	$f = 1 \text{ MHz}$	-	1.3	-	Ω
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25 A; V_{DS} = 20 V; V_{GS} = 10 V;$ <a href="#">Fig. 12; Fig. 13</a>	-	127	-	nC
		$I_D = 25 A; V_{DS} = 20 V; V_{GS} = 4.5 V;$ <a href="#">Fig. 12; Fig. 13</a>	-	59	-	nC
		$I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V$	-	115	-	nC
$Q_{GS}$	gate-source charge	$I_D = 25 A; V_{DS} = 20 V; V_{GS} = 4.5 V;$ <a href="#">Fig. 12; Fig. 13</a>	-	19	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	12	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	8	-	nC
$Q_{GD}$	gate-drain charge		-	17	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 A; V_{DS} = 20 V;$ <a href="#">Fig. 12; Fig. 13</a>	-	2.7	-	V
$C_{iss}$	input capacitance	$V_{DS} = 20 V; V_{GS} = 0 V; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 14</a>	-	8845	-	pF
$C_{oss}$	output capacitance		-	1878	-	pF
$C_{rss}$	reverse transfer capacitance		-	382	-	pF

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$t_{d(on)}$	turn-on delay time	$V_{DS} = 20\text{ V}; R_L = 0.8\ \Omega; V_{GS} = 4.5\text{ V}; R_{G(ext)} = 5\ \Omega$	-	52	-	ns	
$t_r$	rise time		-	62	-	ns	
$t_{d(off)}$	turn-off delay time		-	65	-	ns	
$t_f$	fall time		-	38	-	ns	
$Q_{oss}$	output charge	$V_{GS} = 0\text{ V}; V_{DS} = 20\text{ V}; f = 1\text{ MHz}; T_j = 25\text{ }^\circ\text{C}$	-	51	-	nC	
<b>Source-drain diode</b>							
$V_{SD}$	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C}; \text{Fig. 15}$	-	0.78	1.2	V	
$t_{rr}$	reverse recovery time	$I_S = 25\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V}; V_{DS} = 20\text{ V}; \text{Fig. 16}$	-	48	-	ns	
$Q_r$	recovered charge		[1]	-	67	-	nC
$t_a$	reverse recovery rise time		-	-	28.6	-	ns
$t_b$	reverse recovery fall time		-	-	23.8	-	ns

[1] includes capacitive recovery



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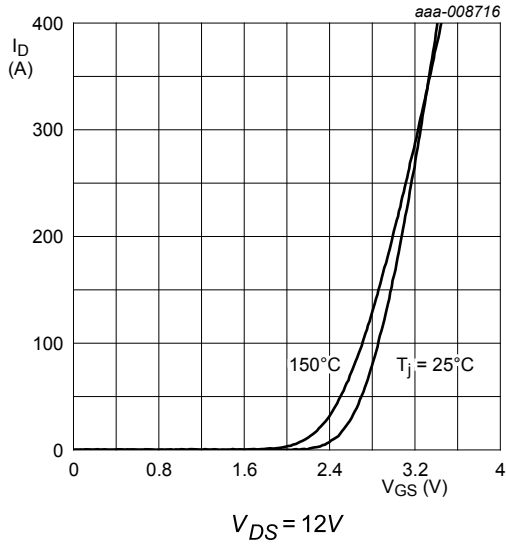


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

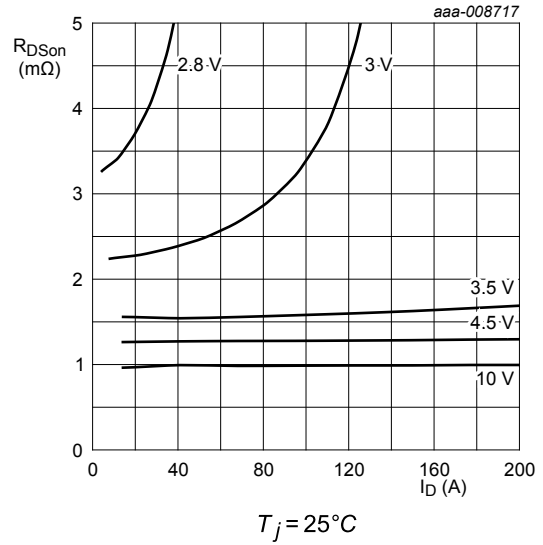


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values

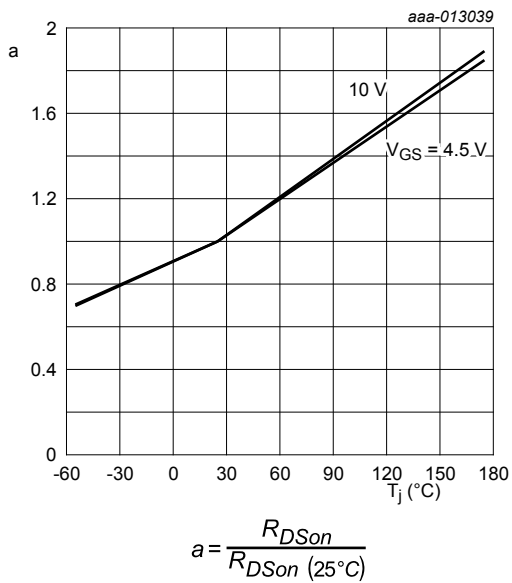


Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

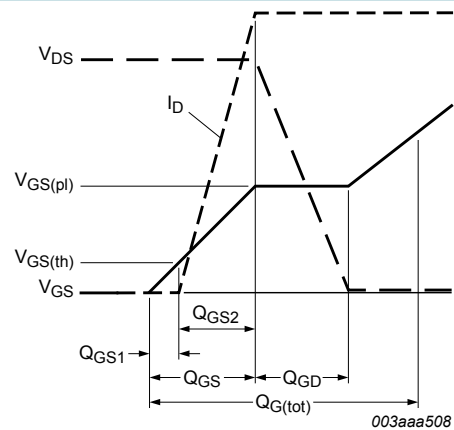


Fig. 12. Gate charge waveform definitions



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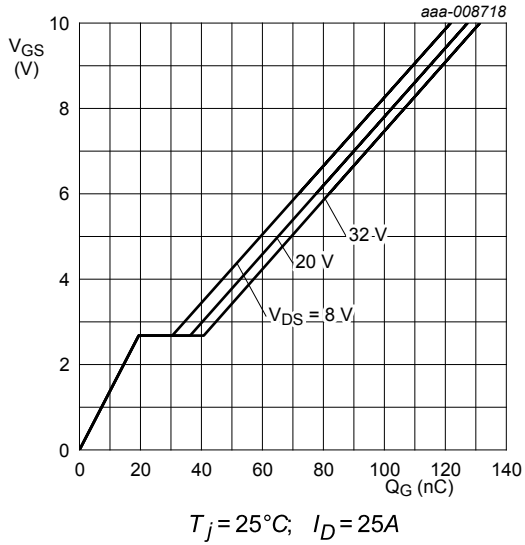


Fig. 13. Gate-source voltage as a function of gate charge; typical values

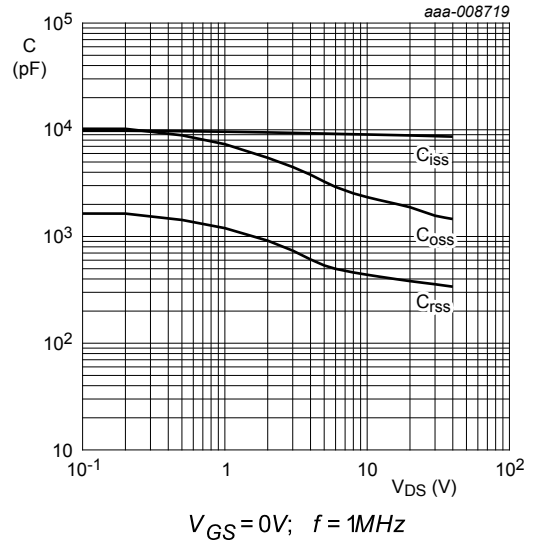


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

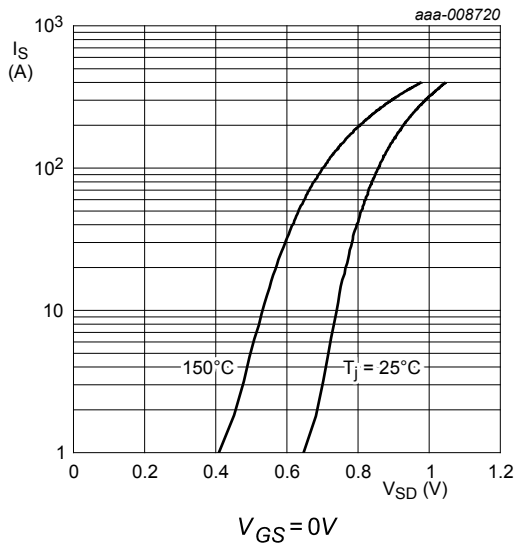


Fig. 15. Source current as a function of source-drain voltage; typical values

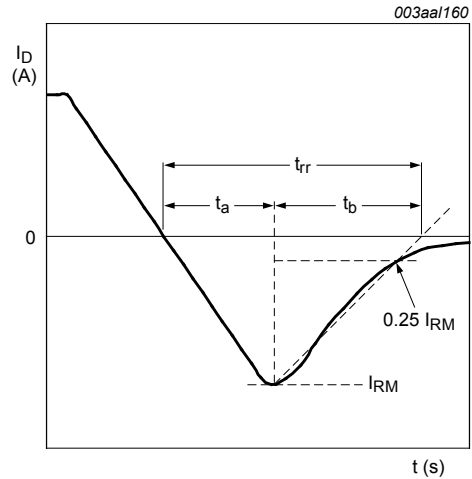


Fig. 16. Reverse recovery timing definition

### 11. Package outline

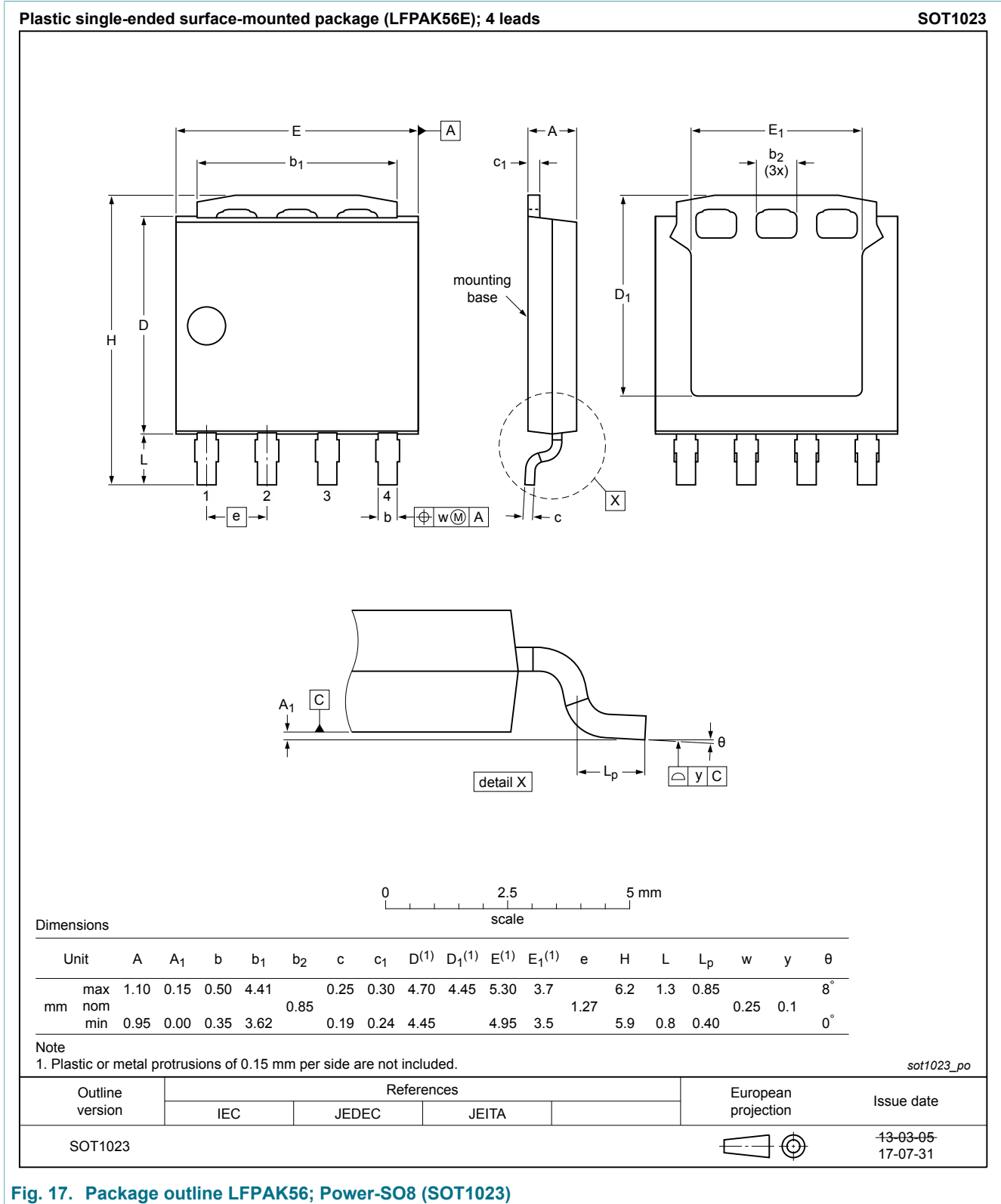


Fig. 17. Package outline LPAK56; Power-SO8 (SOT1023)

## 12. Soldering

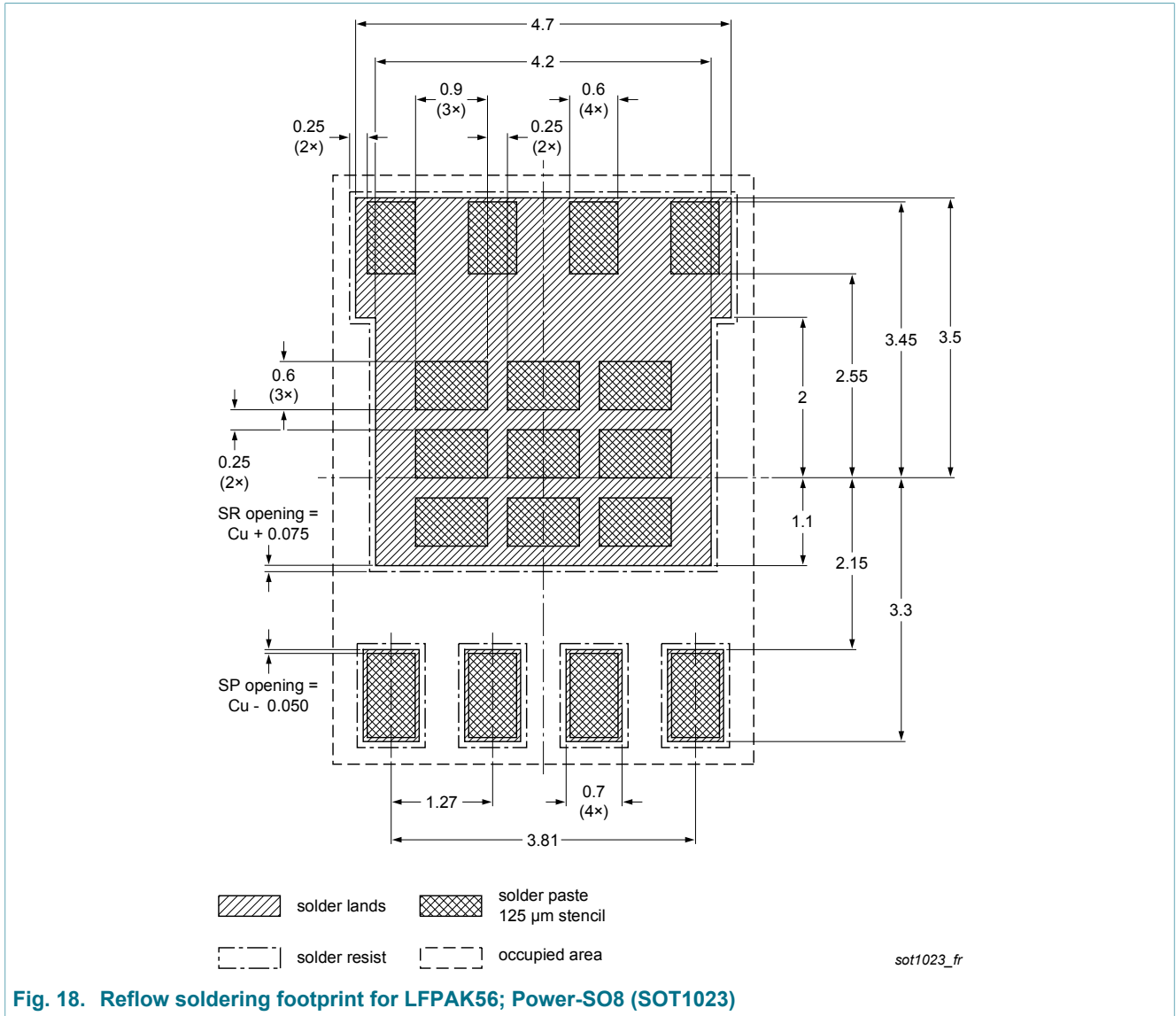


Fig. 18. Reflow soldering footprint for LPAK56; Power-SO8 (SOT1023)

## N-channel 40 V, 1.1 mΩ, 280 A logic level MOSFET in LPAK56 using NextPower-S3 Schottky-Plus technology

### 13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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