GENERAL DESCRIPTION

OB2365T combines a dedicated current mode PWM controller with a high voltage power MOSFET. It is optimized for high performance, low standby power, and cost effective off-line flyback converter applications.

At normal load condition, it operates in QR mode in high line input voltage. To minimize switching loss, the maximum switching frequency in QR mode is internally limited to 77 KHz. When the loading goes low, it operates in PFM mode with valley switching for high power conversion efficiency. When the load is very small, the IC operates in 'Extended Burst Mode' to minimize the standby power loss. Additionally, in the low line input voltage, the IC operates in fixed frequency (65KHz) CCM mode at the heavy loading. As a result, high conversion efficiency can be achieved in the whole loading range.

VDD low startup current and low operating current contribute to a reliable power on startup and low standby design with OB2365T.

OB2365T offers comprehensive protection coverage with auto-recovery including Cycle-by-Cycle current limiting (OCP), over load protection (OLP), VDD under voltage lockout (UVLO), external over temperature protection (OTP), and over voltage protection (OVP). Excellent EMI performance is achieved with On-Bright proprietary frequency shuffling technique.

The tone energy at below 23KHz is minimized in the design and audio noise is eliminated during operation.

OB2365T is offered in DIP8 package.

APPLICATIONS

Offline AC/DC flyback converter for

- General power supply
- Power Adapter

FEATURES

- Power on soft start reducing MOSFET Vds stress
- Multi-Mode Operation

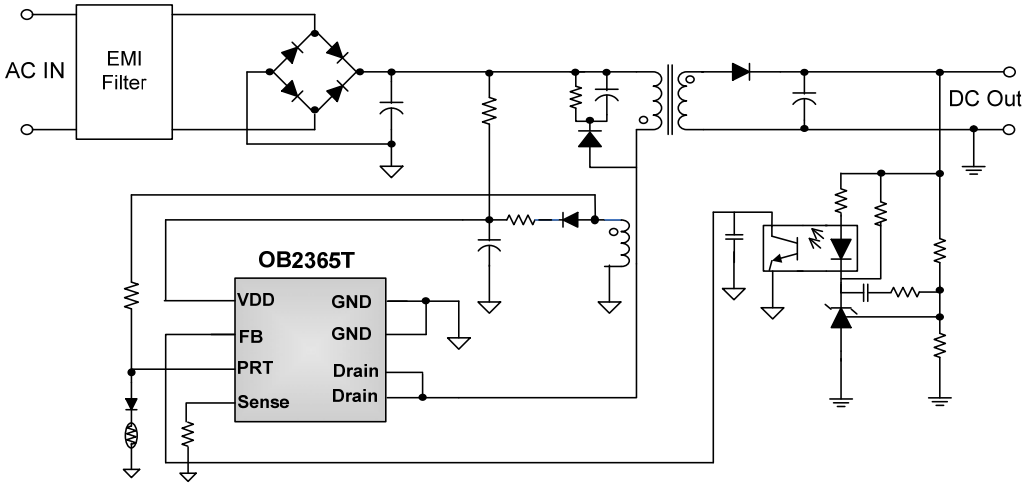
  77KHz maximum clamping frequency in QR mode @ Full Load in high line voltage

  65KHz minimum clamping frequency in CCM mode @ Heavy Load in low line voltage

  Valley switching operation @ Green mode

  Burst Mode @ Light Load & No Load
- Frequency shuffling for EMI
- Extended burst mode control for improved efficiency and low standby power design
- Audio noise free operation
- Comprehensive protection coverage
  - o VDD Under Voltage Lockout with hysteresis (UVLO)
  - o VDD Over Voltage Protection (VCC OVP)
  - o Cycle-by-cycle over current threshold setting for constant output power limiting over universal input voltage range
  - o Over Load Protection (OLP) with auto-recovery
  - o External (if NTC resistor is connected at DEM pin)or internal Over Temperature Protection (OTP) with auto-recovery
  - o Output Over Voltage Protection(Output OVP) with auto-recovery, and the OVP triggered voltage can be adjusted by the resistor connected between auxiliary winding and DEM pin
  - o Output diode short protection with auto-recovery

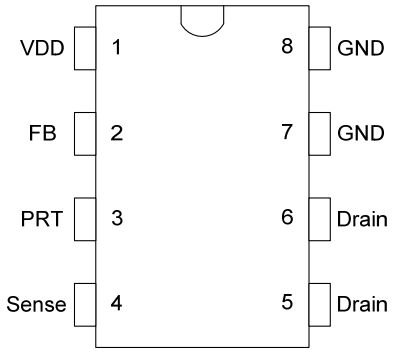
TYPICAL APPLICATION



GENERAL INFORMATION

Pin Configuration

The OB2365T is offered in DIP8 package as shown below.



Ordering Information

Part Number	Description
OB2365TAP	DIP8, Halogen-free in tube

Package Dissipation Rating

Package	RθJA (℃/W)
DIP8	75

Note: Drain Pin Connected to 100mm^2 PCB copper clad.

Absolute Maximum Ratings

Parameter	Value
Drain voltage (off state)	-0.3V to BVdss
VDD voltage	29.5V
PRT input voltage	-0.3V to 7V
FB input voltage	-0.3 to 7V
Sense input voltage	-0.3 to 7V
Min/Max operating junction temperature T_J	-40 to 150℃
Min/Max storage temperature T_{stg}	-55 to 150℃
Lead temperature (soldering, 10secs)	260℃

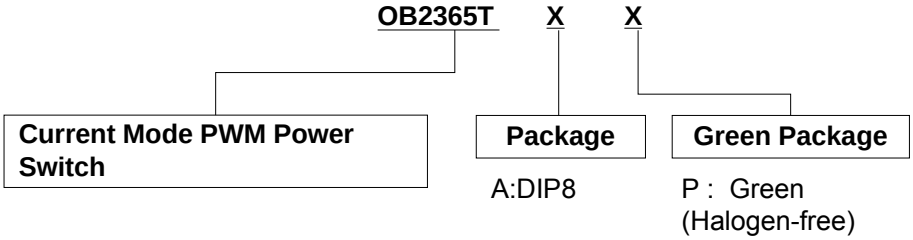
Note: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

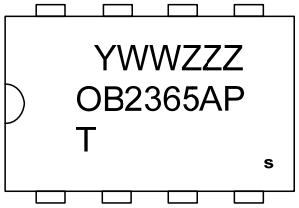
Output Power Table

Product	230VAC±15% Adapter[1]	85-265VAC Adapter[1]
OB2365T	29W	24W

Notes: 1. Maximum practical continuous power in an adapter design with sufficient drain pattern as a heat sink, at 40℃ ambient.

Marking Information



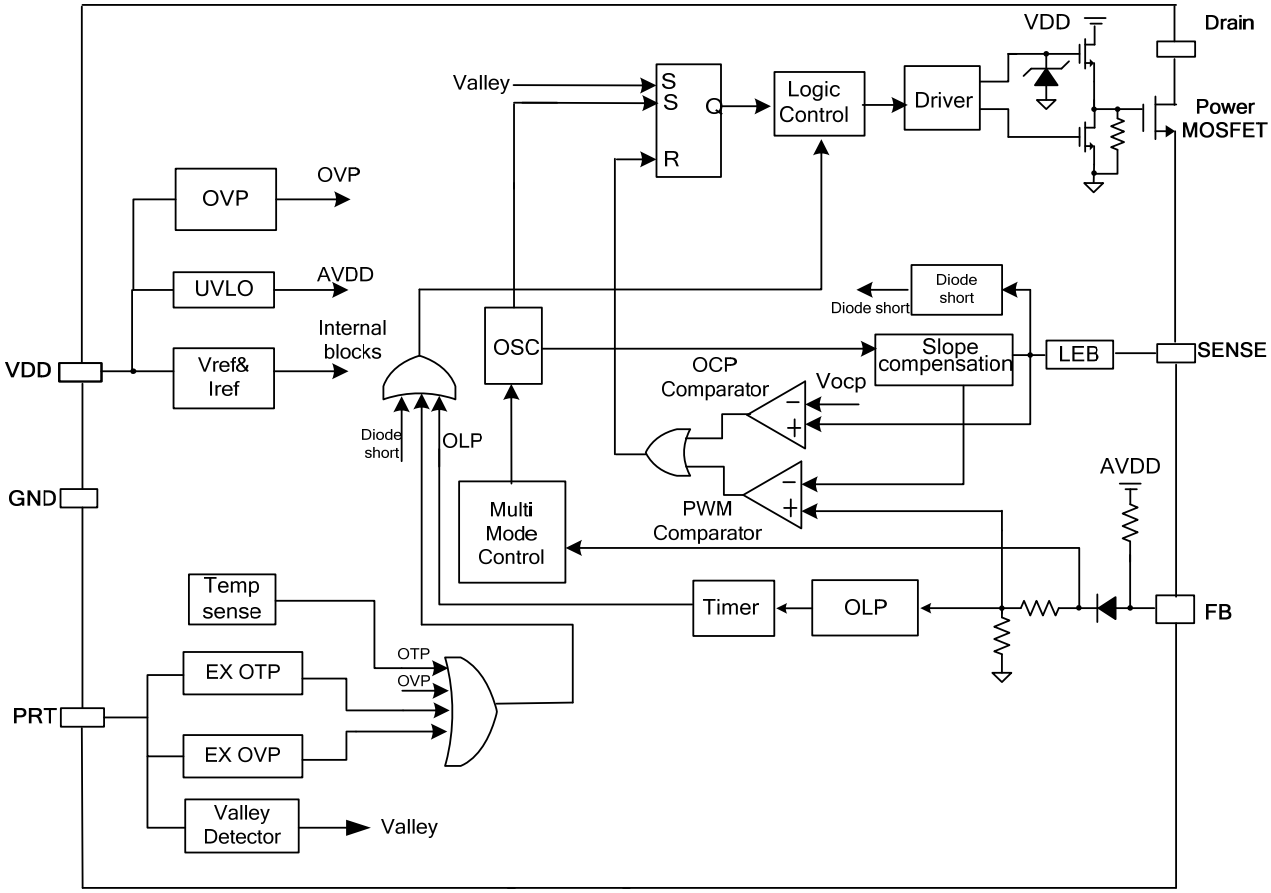


Y:Year Code
WW:Week Code(01-52)
ZZZ:Lot Code
A:DIP8 Package
P:Green Package(Halogen-free)
T:Character Code
s:Internal Code(Optional)

TERMINAL ASSIGNMENTS

Pin Name	I/O	Description
GND	P	Ground
FB	I	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and the current-sense signal at Pin 4
PRT	I	Multiple functions pin. Connecting a NTC resistor to ground for OTP detection. Connecting a resistor from Vaux can adjust OVP trigger voltage and detect transformer core demagnetization. If both OTP and OVP are needed, a diode should be connected between DEM pin and the NTC resistor.
Sense	I	Current sense input
VDD	P	IC DC power supply Input
Drain	O	HV MOSFET drain pin. The drain pin is connected to the primary lead of the transformer

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

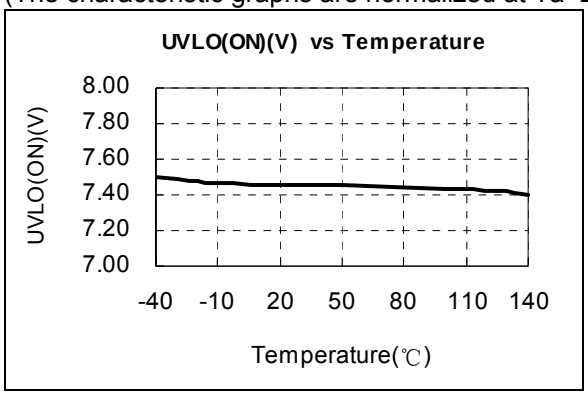
(T_A = 25℃, VDD=18V, unless otherwise noted)

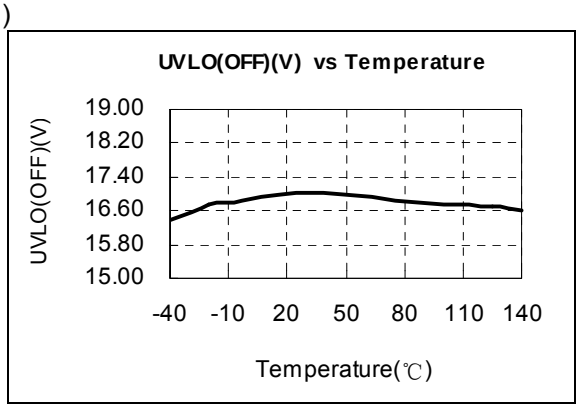
Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
Supply Voltage (VDD)						
Istartup	VDD Start up Current	VDD=UVLO(OFF)-1V, measure leakage current into VCC		2	5	uA
I_VDD_Operation	Operation Current	VDD=18V,CS=4V, FB=3.5V,measure I(VCC)		2	3	mA
I_VDD_Burst	Burst Current	CS=0V,FB=0.5V, measure I(VCC)		0.3	0.5	mA
UVLO(ON)	VDD Under Voltage Lockout Enter		6.8	7.3	7.8	V
UVLO(OFF)	VDD Under Voltage Lockout Exit (Recovery)		16	17	18	V
Vpull-up	Pull-up PMOS active			10		V
OVP	VDD Over Voltage Protection threshold voltage	FB=3V,CS=0V. Slowly ramp VCC, until no gate switching.	26.5	28	29.5	V
Feedback Input Section(FB Pin)						
V_{FB} Open	V_{FB} Open Loop Voltage			5.1		V
Avcs	PWM input gain ΔVFB/ΔVCS			3.3		V/V
Maximum duty cycle	Max duty cycle @ VDD=18V,VFB=3V,VCS=0V		75	80	85	%
Vref_green	The threshold enter green mode			2.1		V
Vref_burst_H	The threshold exits burst mode			1.33		V
Vref_burst_L	The threshold enters burst mode			1.23		V
I_{FB}_Short	FB pin short circuit current	Short FB pin to GND and measure current		0.16		mA
V_{TH}_OLP	Open loop protection, FB Threshold Voltage			4.4		V
Td_OLP	Open loop protection, Debounce Time			60		ms
Z_{FB}_IN	Input Impedance			30		KΩ
Current Sense Input(CS Pin)						
SST_CS	Soft start time for CS peak			2.5		ms
T_blanking	Leading edge blanking time			330		ns
Td_OC	Over Current Detection and Control Delay	From Over Current Occurs till the Gate driver output start to turn off		80		ns
V_{TH}_OC	Internal Current Limiting Threshold Voltage with zero duty cycle			0.5		V
V_{TH}_OC_Clamp	OCP CS voltage clamper			0.72		V
PRT pin						
IRT	Output current for external OTP		94	100	106	uA

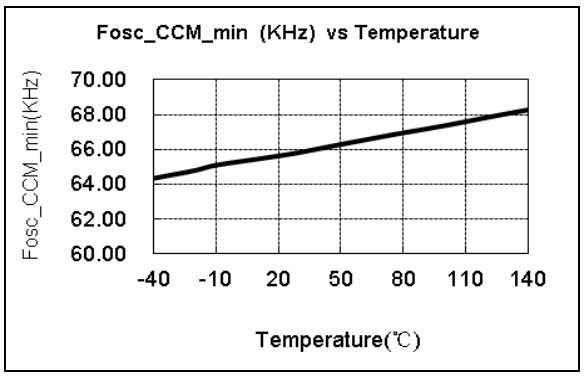
	detection					
VOTP	Threshold voltage for external OTP		0.85	0.90	0.95	V
T_{d_OTP}	External OTP debounce time			60		Cycles
Ioutput_ovp	Current threshold for adjustable output OVP		170	180	190	uA
Td_output_ovp	Output OVP debounce time			7		Cycles
In-chip OTP						
OTP enter				150		℃
OTP exit				120		℃
Oscillator						
Fosc_max_QR	Average max clamp oscillation frequency in QR mode	VDD=15V, FB=3V,		77		KHz
∆f_OSC_max_QR	Max clamp oscillation frequency jittering			±7		%
Fosc_min_CCM	Min clamp oscillation frequency in CCM mode	VDD=15V,FB=3V,		65		KHz
∆f_OSC_CCM	Min clamp oscillation frequency jittering			±7		%
F_shuffling	Shuffling frequency			240		Hz
∆f_Temp	Frequency Temperature Stability			1		%
∆f_VCC	Frequency Voltage Stability			1		%
F_Burst	Burst Mode Switch Frequency			23		KHz
Mosfet section						
BVdss	MOSFET drain-source breakdown voltage		600			V
Rdson	Static drain to source on resistance			1.6		Ω

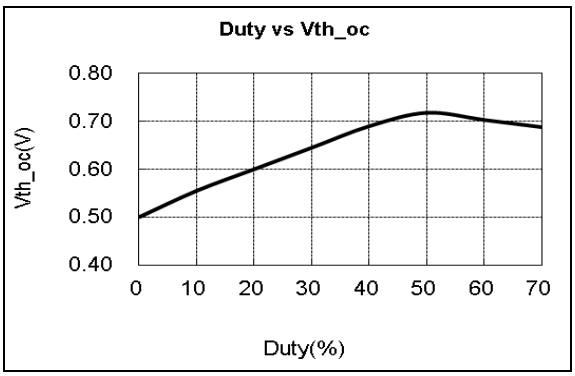
CHARACTERIZATION PLOTS

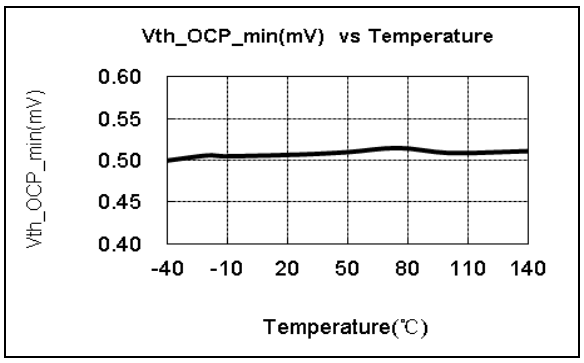
(The characteristic graphs are normalized at Ta=25℃)

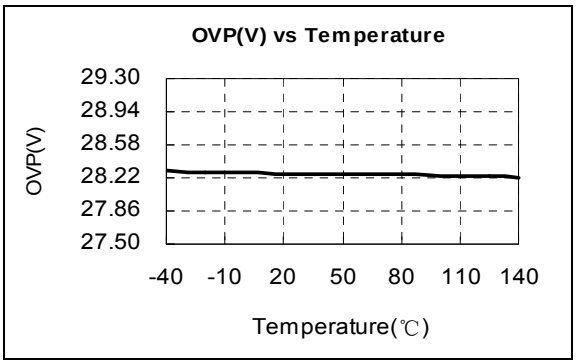


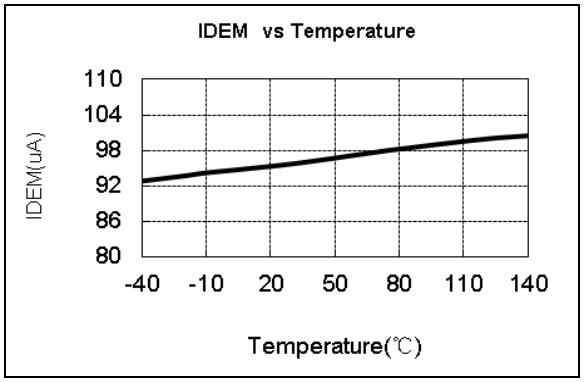


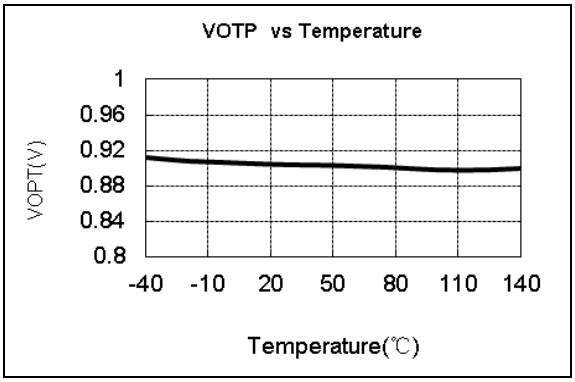












OPERATION DESCRIPTION

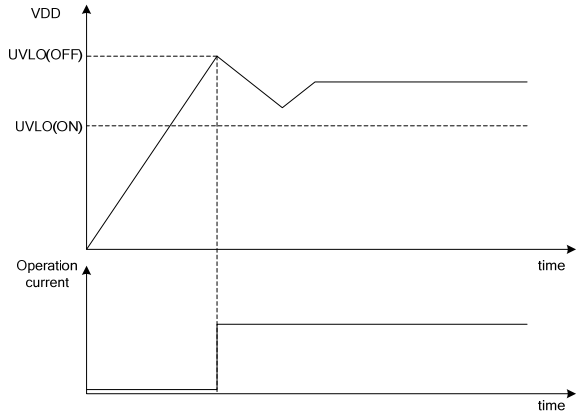
OB2365T is a highly integrated current mode PWM control IC optimized for high performance, low standby power and cost effective offline flyback converter applications. The 'extended burst mode' control greatly reduces the standby power consumption and helps the design easier to meet the international power conservation requirements.

Startup Current and Start up Control

Startup current of OB2365T is designed to be very low so that VDD could be charged up above UVLO threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet achieve a reliable startup in application.

Operating Current

The Operating current of OB2365T is low at 2mA (typical). Good efficiency is achieved with OB2365T low operation current together with the 'extended burst mode' control features.

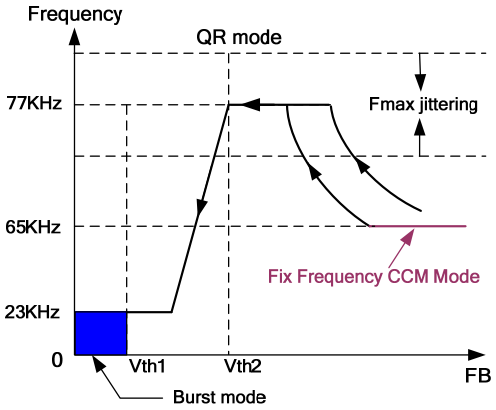


Soft Start

OB2365T features an internal 2.5ms (typical) soft start to soften the electrical stress occurring in the power supply during startup. It is activated during the power on sequence. As soon as VCC reaches UVLO(OFF), the CS peak voltage is gradually increased from 0.05V to the maximum level. Every restart up is followed by a soft start.

Multi Mode Operation for High Efficiency

OB2365T is a multi-mode QR/PWM controller. The controller changes the mode of operation according to line voltage and load conditions.



At full load conditions, there are two situations: firstly, if the system input is in low line input range, the IC operates in 65K fixed frequency CCM mode. Thus, small size transformer can be used with high power conversion efficiency. Secondly, if the system input is in high line input range, the IC operates in QR mode. In this way, high power conversion efficiency can be achieved in the universal input range when system is at full loading conditions.

At normal operating conditions (Vth2<VFB), the system operates in QR mode. The frequency varies depending on the line voltage and the load conditions. Therefore, the system may actually work in DCM when the average 77KHz frequency clamping is reached.

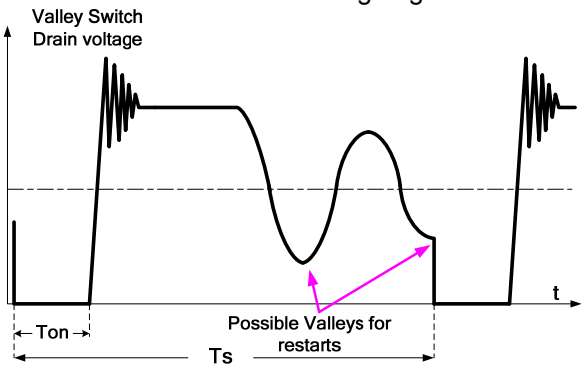
At light load conditions (Vth1<VFB<Vth2), the system operates in PFM (pulse frequency modulation) mode for high power conversion efficiency. Generally, in flyback converter, the decreasing of load results in voltage level decreasing at FB pin. The controller monitors the voltage level at FB and control the switching frequency. However, the valley switching characteristic is still preserved in PFM mode. That is, when load decreases, the system automatically skip more and more valleys and the switching frequency is thus reduced. In such way, a smooth frequency fold-back is realized and high power conversion efficiency is achieved.

At no load or very light load conditions (VFB<Vth1), the system operates in On-Bright's proprietary "extended burst mode". In the extended burst mode, the switching frequency at below 23KHz is minimized to avoid audio noise during operation.

Demagnetization Detection

The transformer core demagnetization is detected by monitoring the voltage activity on the auxiliary windings through PRT pin. This voltage features a flyback polarity. After the on time (determined by the CS voltage and FB voltage), the switch is off and the flyback stroke starts. After the flyback stroke, the drain voltage shows an oscillation with a frequency of approximately $1/2\pi\sqrt{L_pC_d}$, where L_p is the primary self inductance of primary winding of the transformer and C_d is the capacitance on the drain node.

The typical detection level is fixed at -50mV at the PRT pin. Demagnetization is recognized by detection of a possible "valley" when the voltage at PRT is below -50mV in falling edge.



Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting is offered in OB2365T current mode PWM control. The switch current is detected by a sense resistor into the sense pin. An internal leading edge blanking circuit chops off the sensed voltage spike at initial internal power MOSFET on state due to snubber diode reverse recovery and surge gate current of internal power MOSFET so that the external RC filtering on sense input is no longer needed. The current limiting comparator is disabled and cannot turn off the internal power MOSFET during the blanking period. The PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

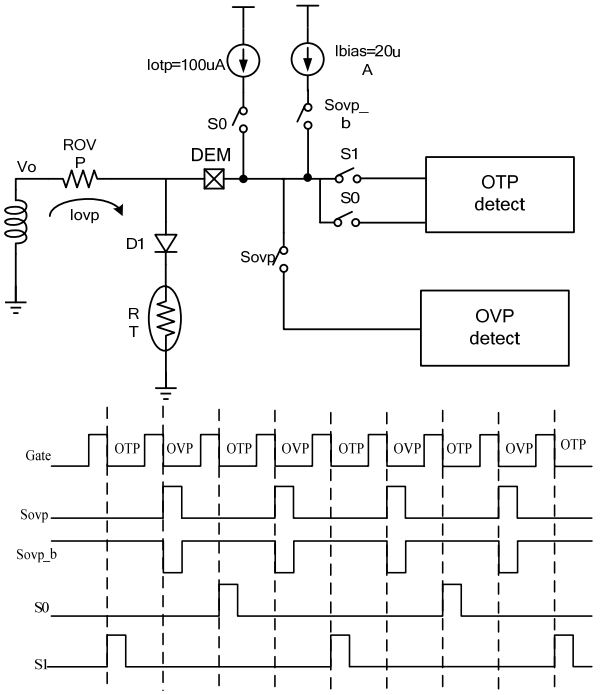
Internal Synchronized Slope Compensation

Built-in slope compensation circuit adds voltage ramp into the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

Driver

The internal power MOSFET in OB2365T is driven by a dedicated gate driver for power switch control. A too weak the gate drive strength results in higher conduction and switch loss of MOSFET while too strong gate drive results in the compromise of EMI.

Dual Function of External OTP and Output OVP



On-Bright proprietary dual function of external OTP and output OVP provides feasible and accurate detection of external OTP through NTC resistor and output OVP. The dual function is realized through time-division technology as shown in the figure.

For external OTP detection, when switch control signal S1= "1", about 20uA (typical) current flows out from PRT pin. When switch control signal S0= "1",about 120uA (typical) current flows out from DEM pin. The DEM pin voltage difference △Votp at phase S0 and S1 phase is equal to $\Delta V_{OTP} = \frac{RT \cdot ROVP}{ROVP + RT} \cdot 100uA \cdot$

When △Votp<0.9V , external OTP auto-recovery protection is triggered after 60 Gate cycles debounce.

For output OVP detection, when Sovp= "1", Iovp is equal to Vo/ROVP. If Iovp is larger than 180uA (typical), OVP auto-recovery protection is triggered after 7 Gate cycles debounce. By selecting proper Rovp resistance, output OVP level can be programmed.

$$\frac{Vout * \frac{Naux}{Nout} - 0.15V}{Rovp} \geq 180uA$$

Vout: Output voltage
Nout: The secondary winding turns
Naux: The auxiliary winding turns

Protection Controls

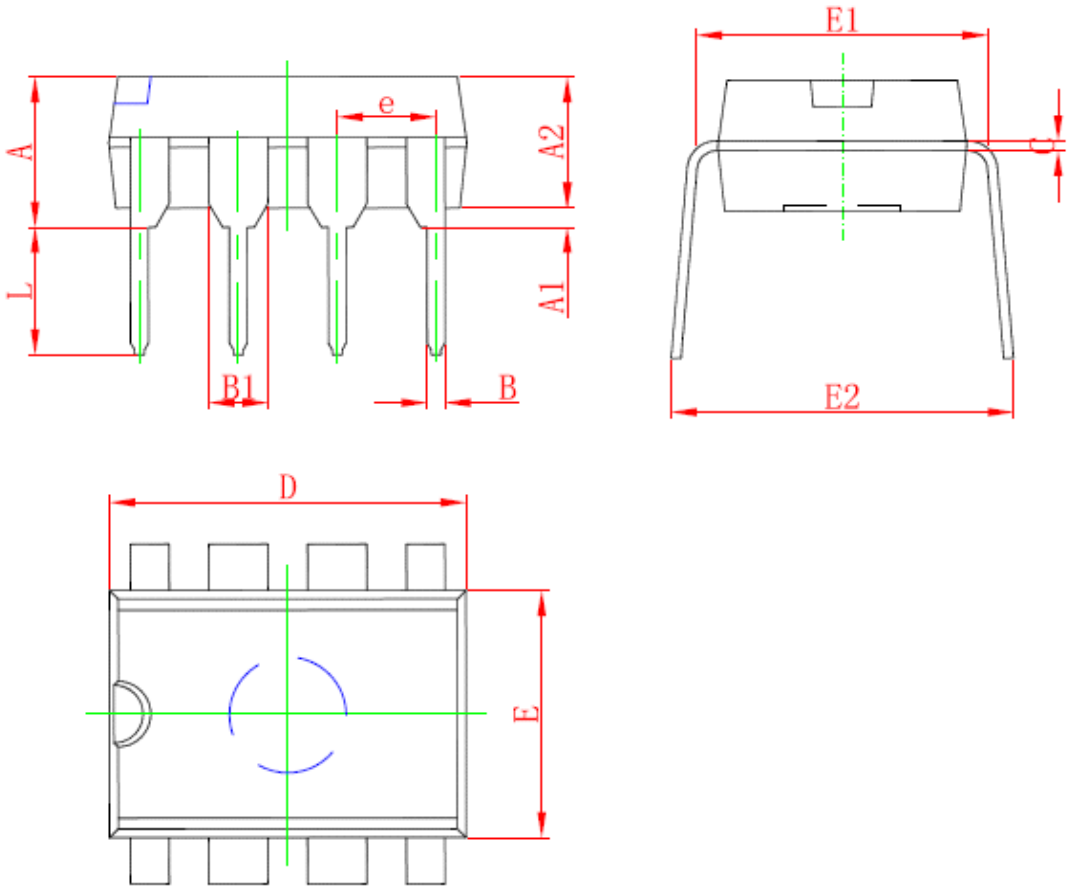
Good power supply system reliability is achieved with auto-recovery protection features including Cycle-by-Cycle current limiting (OCP), Under Voltage Lockout on VDD (UVLO), Over Temperature Protection (OTP), VCC and output Over Voltage Protection (OVP).

With On-Bright proprietary technology, the OCP is line voltage compensated to achieve constant output power limit over the universal input voltage range.

At overload condition when FB input voltage exceeds power limit threshold value for more than Td_OLP, control circuit reacts to shut down the converter. It restarts when VDD voltage drops below UVLO limit.

PACKAGE MECHANICAL DATA

8-Pin Plastic DIP



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	5.334	0.146	0.210
A1	0.381		0.015	
A2	2.921	4.953	0.115	0.195
B	0.350	0.650	0.014	0.026
B1	1.524 (BSC)		0.06 (BSC)	
C	0.200	0.360	0.008	0.014
D	9.000	10.160	0.354	0.400
E	6.096	7.112	0.240	0.280
E1	7.320	8.255	0.288	0.325
e	2.540 (BSC)		0.1 (BSC)	
L	2.921	3.810	0.115	0.150
E2	7.620	10.920	0.300	0.430

IMPORTANT NOTICE

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