MOSFET

Metal Oxide Semiconductor Field Effect Transistor

CoolMOS™ P6

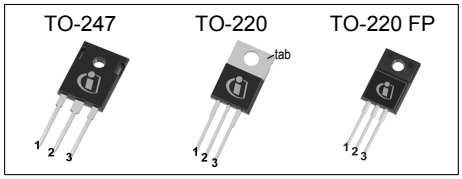
600V CoolMOS™ P6 Power Transistor
IPx60R125P6

Data Sheet

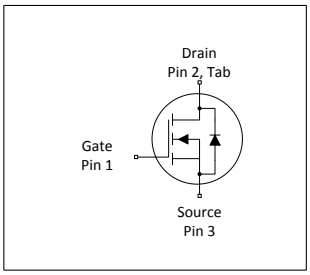
Rev. 2.0
Final

Power Management & Multimarket

1 Description



CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. CoolMOS™ P6 series combines the experience of the leading SJ MOSFET supplier with high class innovation. The offered devices provide all benefits of a fast switching SJ MOSFET while not sacrificing ease of use. Extremely low switching and conduction losses make switching applications even more efficient, more compact, lighter and cooler.



Features

- Increased MOSFET dv/dt ruggedness
- Extremely low losses due to very low FOM Rdson*Qg and Eoss
- Very high commutation ruggedness
- Easy to use/drive
- Pb-free plating, Halogen free mold compound
- Qualified for industrial grade applications according to JEDEC (J-STD20 and JESD22)

Applications

PFC stages, hard switching PWM stages and resonant switching stages for e.g. PC Silverbox, Adapter, LCD & PDP TV, Lighting, Server, Telecom and UPS.

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS} @ $T_{j,max}$	650	V
$R_{DS(on),max}$	125	mΩ
$Q_{g.typ}$	56	nC
$I_{D,pulse}$	87	A
E_{oss}@400V	7.2	µJ
Body diode di/dt	300	A/µs

Type / Ordering Code	Package	Marking	Related Links
IPW60R125P6	PG-TO 247	6R125P6	see Appendix A
IPP60R125P6	PG-TO 220		
IPA60R125P6	PG-TO 220 FullPAK		

Table of Contents

2 Maximum ratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current [1]	I_D	- -	- -	30.0 19.0	A	T_C=25°C T_C=100°C
Pulsed drain current [2]	$I_{D,pulse}$	-	-	87	A	T_C=25°C
Avalanche energy, single pulse	E_{AS}	-	-	636	mJ	I_D=5.2A; V_{DD}=50V; see table 10
Avalanche energy, repetitive	E_{AR}	-	-	0.96	mJ	I_D=5.2A; V_{DD}=50V; see table 10
Avalanche current, repetitive	I_{AR}	-	-	5.2	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	100	V/ns	V_{DS}=0...400V
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC (f>1 Hz)
Power dissipation (Non FullPAK) TO-220, TO-247	P_{tot}	-	-	219	W	T_C=25°C
Power dissipation (FullPAK) TO-220FP	P_{tot}	-	-	34	W	T_C=25°C
Storage temperature	T_{stg}	-55	-	150	°C	-
Operating junction temperature	T_j	-55	-	150	°C	-
Mounting torque (Non FullPAK) TO-220, TO-247	-	-	-	60	Ncm	M3 and M3.5 screws
Mounting torque (FullPAK) TO-220FP	-	-	-	50	Ncm	M2.5 screws
Continuous diode forward current	I_S	-	-	26.0	A	T_C=25°C
Diode pulse current [2]	$I_{S,pulse}$	-	-	87	A	T_C=25°C
Reverse diode dv/dt [3]	dv/dt	-	-	15	V/ns	V_{DS}=0...400V, I_{SD}<=I_S, T_j=25°C see table 8
Maximum diode commutation speed	di_f/dt	-	-	300	A/µs	V_{DS}=0...400V, I_{SD}<=I_S, T_j=25°C see table 8
Insulation withstand voltage for TO-220FP	V_{ISO}	-	-	2500	V	V_{rms}, T_C=25°C, t=1min

[1] Limited by $T_{j\,max}$. Maximum duty cycle D=0.75
[2] Pulse width t_p limited by $T_{j,max}$
[3] Identical low side and high side switch with identical R_G

3 Thermal characteristics

Table 3 Thermal characteristics (Non FullPAK) TO-220, TO-247

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.57	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	leaded
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6mm (0.063 in.) from case for 10s

Table 4 Thermal characteristics (FullPAK) TO-220FP

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	3.65	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	80	°C/W	leaded
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6mm (0.063 in.) from case for 10s

4 Electrical characteristics

at T_j=25°C, unless otherwise specified

Table 5 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	V_{GS}=0V, I_D=1mA
Gate threshold voltage	$V_{(GS)th}$	3.5	4.0	4.5	V	V_{DS}=V_{GS}, I_D=0.96mA
Zero gate voltage drain current	I_{DSS}	- -	- 10	2 -	µA	V_{DS}=600, V_{GS}=0V, T_j=25°C V_{DS}=600, V_{GS}=0V, T_j=150°C
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{GS}=20V, V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	- -	0.113 0.293	0.125 -	Ω	V_{GS}=10V, I_D=11.6A, T_j=25°C V_{GS}=10V, I_D=11.6A, T_j=150°C
Gate resistance	R_G	-	1.7	-	Ω	f=1MHz, open drain

Table 6 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	2660	-	pF	V_{GS}=0V, V_{DS}=100V, f=1MHz
Output capacitance	C_{oss}	-	110	-	pF	V_{GS}=0V, V_{DS}=100V, f=1MHz
Effective output capacitance, energy related [1]	$C_{o(er)}$	-	90	-	pF	V_{GS}=0V, V_{DS}=0...400V
Effective output capacitance, time related [2]	$C_{o(tr)}$	-	398	-	pF	I_D=constant, V_{GS}=0V, V_{DS}=0...400V
Turn-on delay time	$t_{d(on)}$	-	14	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=14.5A, R_G=1.7Ω; see table 9
Rise time	t_r	-	9	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=14.5A, R_G=1.7Ω; see table 9
Turn-off delay time	$t_{d(off)}$	-	44	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=14.5A, R_G=1.7Ω; see table 9
Fall time	t_f	-	5	-	ns	V_{DD}=400V, V_{GS}=13 V, I_D=14.5A, R_G=1.7Ω; see table 9

Table 7 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	16	-	nC	V_{DD}=400V, I_D=14.5A, V_{GS}=0 to 10V
Gate to drain charge	Q_{gd}	-	20	-	nC	V_{DD}=400V, I_D=14.5A, V_{GS}=0 to 10V
Gate charge total	Q_g	-	56	-	nC	V_{DD}=400V, I_D=14.5A, V_{GS}=0 to 10V
Gate plateau voltage	$V_{plateau}$	-	6.1	-	V	V_{DD}=400V, I_D=14.5A, V_{GS}=0 to 10V

[1] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

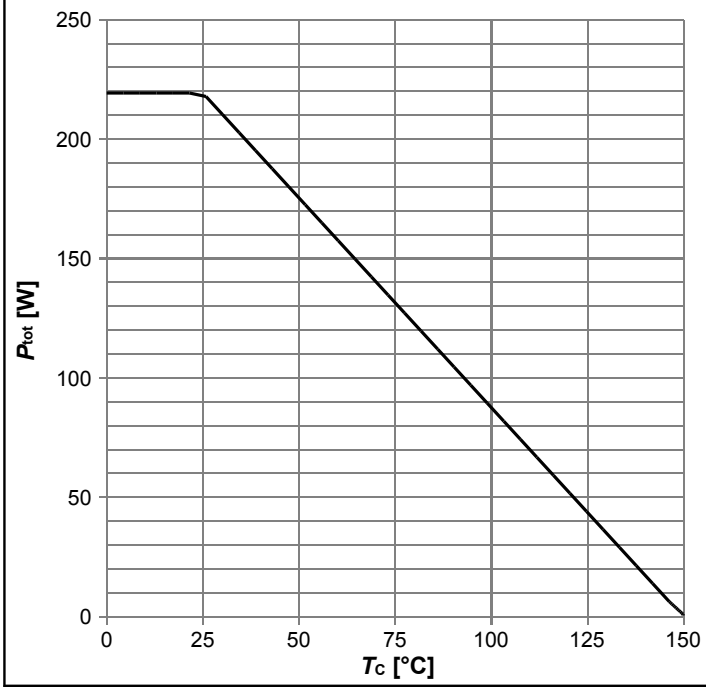
[2] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 8 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	V_{GS}=0V, I_F=14.5A, T_j=25°C
Reverse recovery time	t_{rr}	-	385	-	ns	V_R=400V, I_F=14.5A, di_F/dt=100A/µs; see table 8
Reverse recovery charge	Q_{rr}	-	7	-	µC	V_R=400V, I_F=14.5A, di_F/dt=100A/µs; see table 8
Peak reverse recovery current	I_{rrm}	-	32	-	A	V_R=400V, I_F=14.5A, di_F/dt=100A/µs; see table 8

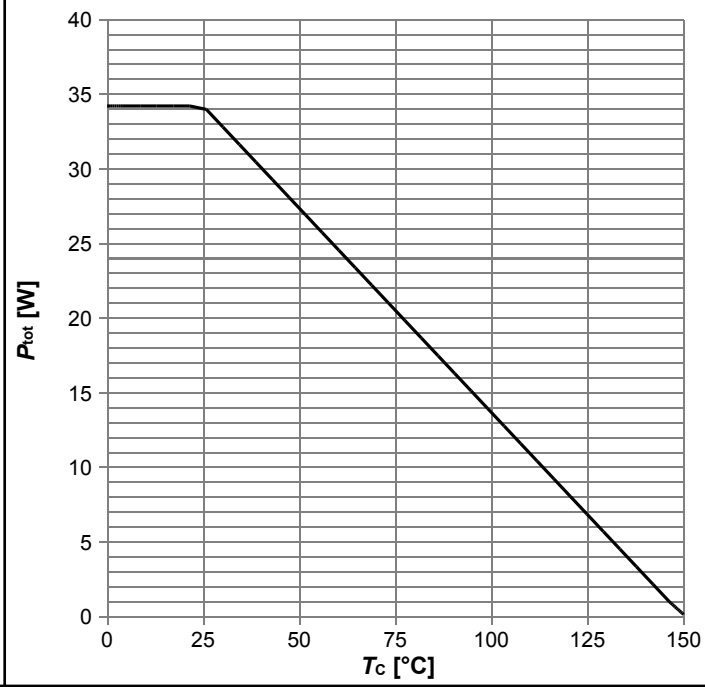
5 Electrical characteristics diagrams

Diagram 1: Power dissipation (Non FullPAK)



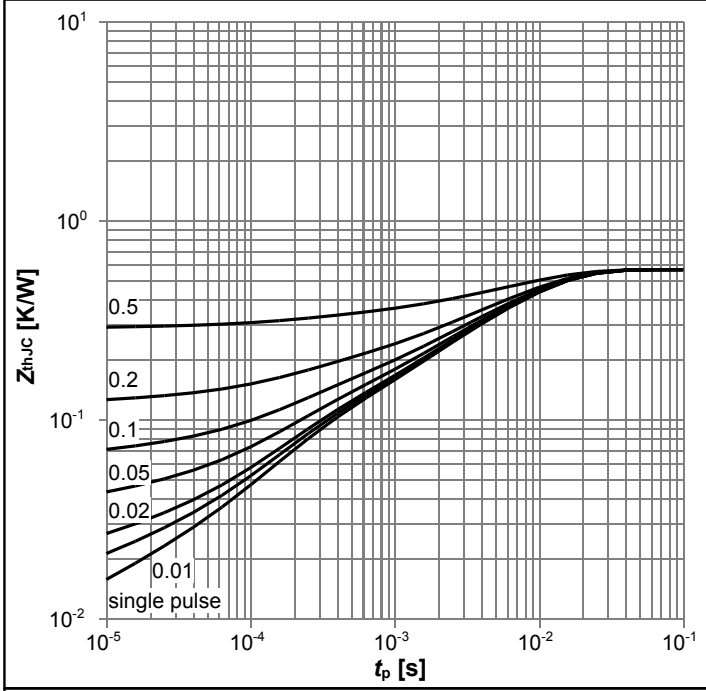
$P_{tot}=f(T_C)$

Diagram 2: Power dissipation (FullPAK)



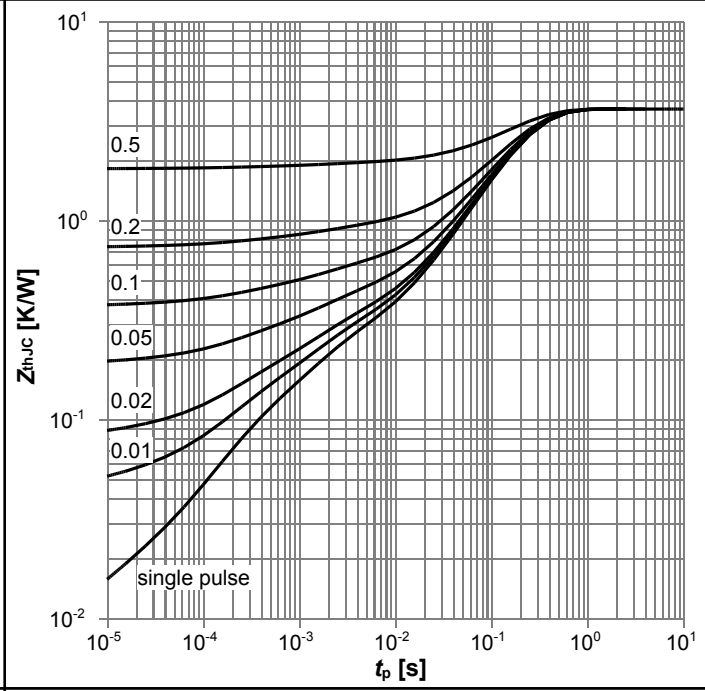
$P_{tot}=f(T_C)$

Diagram 3: Max. transient thermal impedance (Non FullPAK)



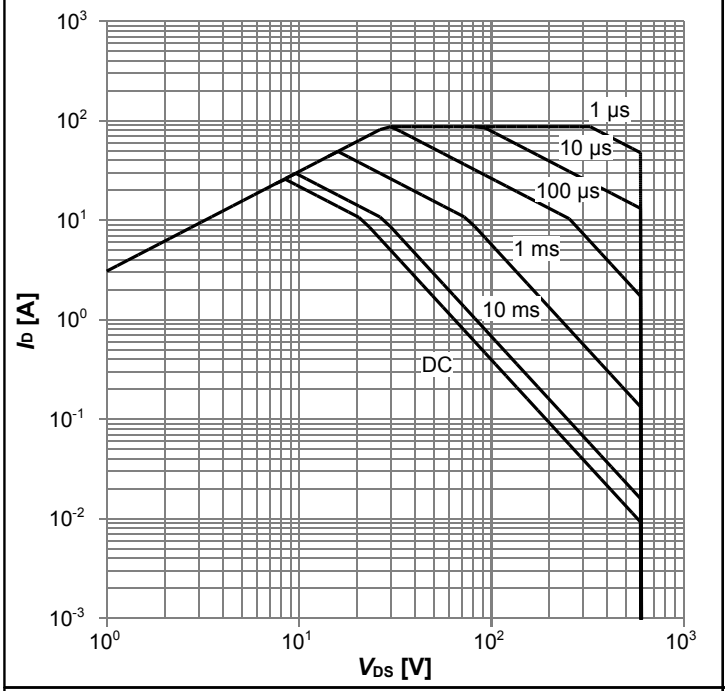
$Z_{thJC}=f(t_P)$; parameter: $D=t_p/T$

Diagram 4: Max. transient thermal impedance (FullPAK)



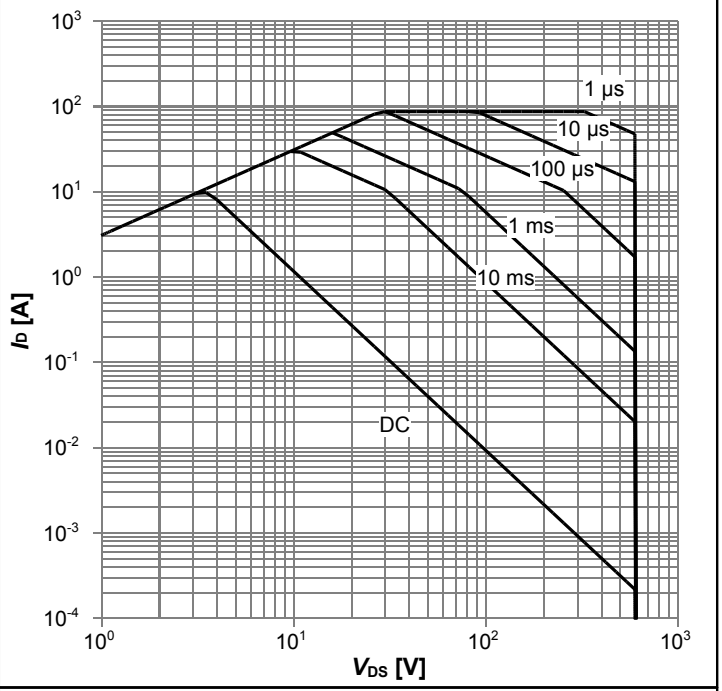
$Z_{thJC}=f(t_P)$; parameter: $D=t_p/T$

Diagram 5: Safe operating area (Non FullPAK)



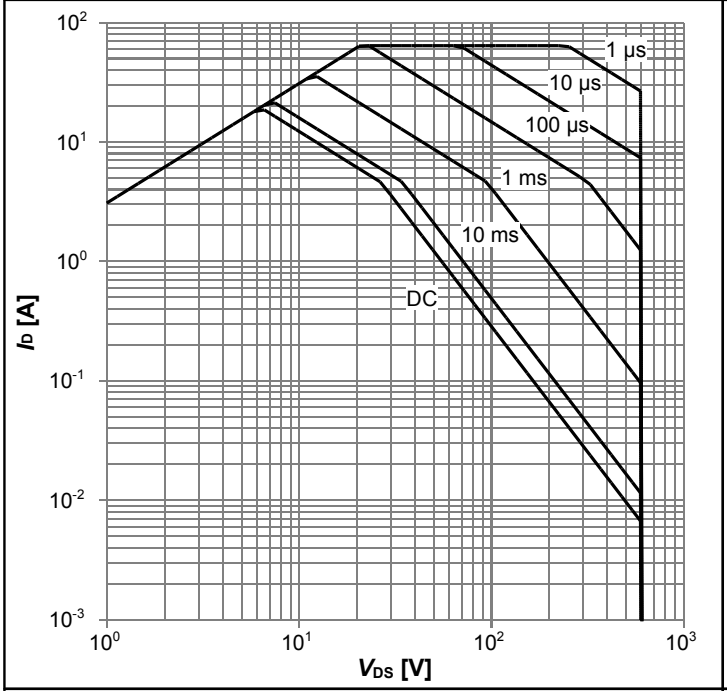
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 6: Safe operating area (FullPAK)



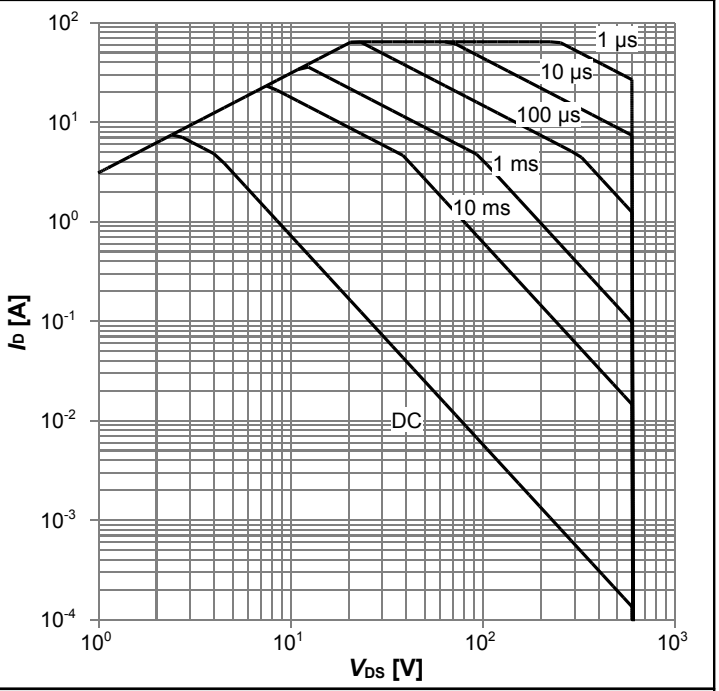
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 7: Safe operating area (Non FullPAK)



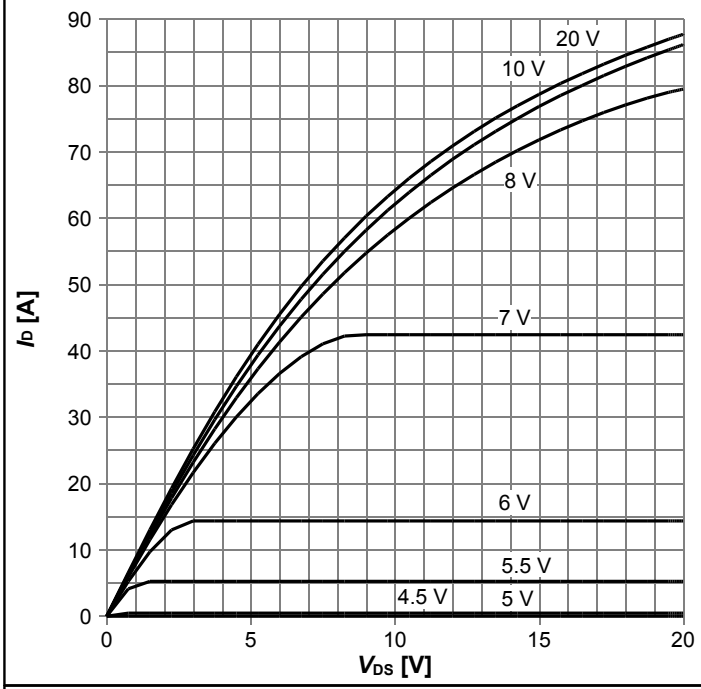
I_D=f(V_{DS}); T_C=80 °C; D=0; parameter: t_p

Diagram 8: Safe operating area (FullPAK)



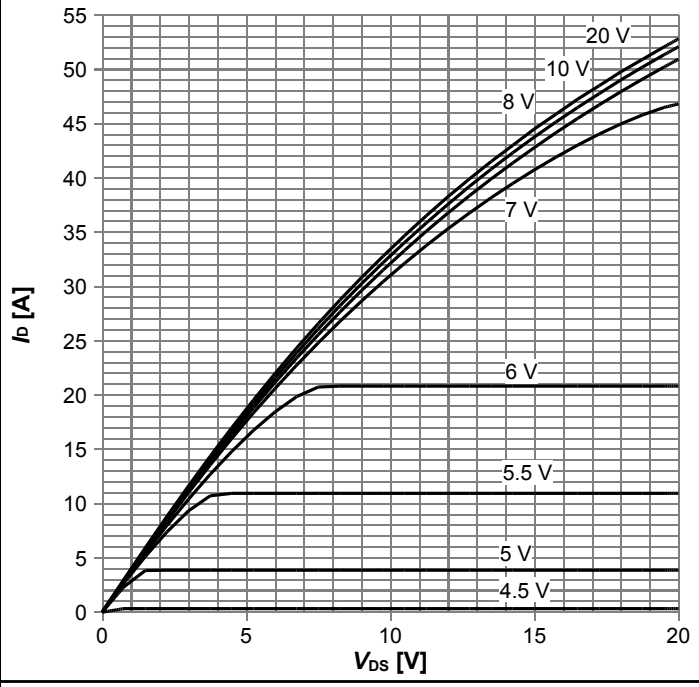
I_D=f(V_{DS}); T_C=80 °C; D=0; parameter: t_p

Diagram 9: Typ. output characteristics



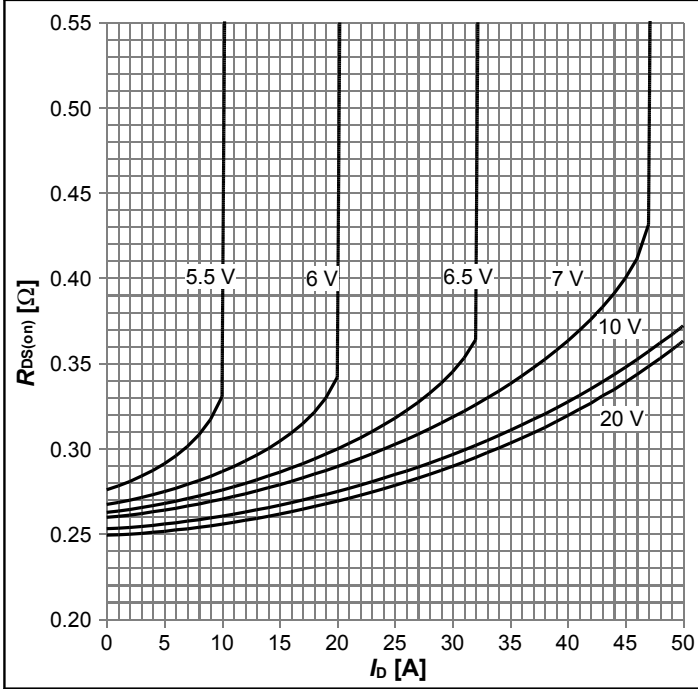
$I_D=f(V_{DS})$; $T_j=25$ °C; parameter: V_{GS}

Diagram 10: Typ. output characteristics



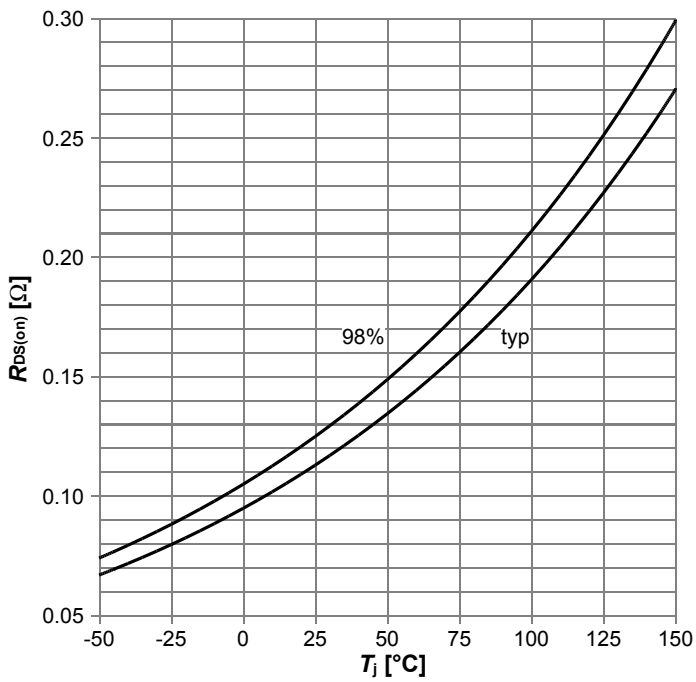
$I_D=f(V_{DS})$; $T_j=125$ °C; parameter: V_{GS}

Diagram 11: Typ. drain-source on-state resistance



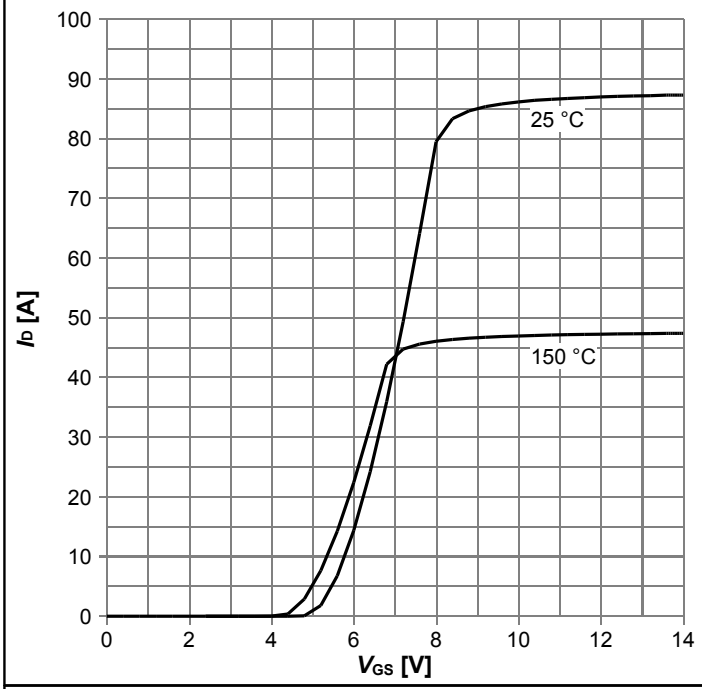
$R_{DS(on)}=f(I_D)$; $T_j=125$ °C; parameter: V_{GS}

Diagram 12: Drain-source on-state resistance



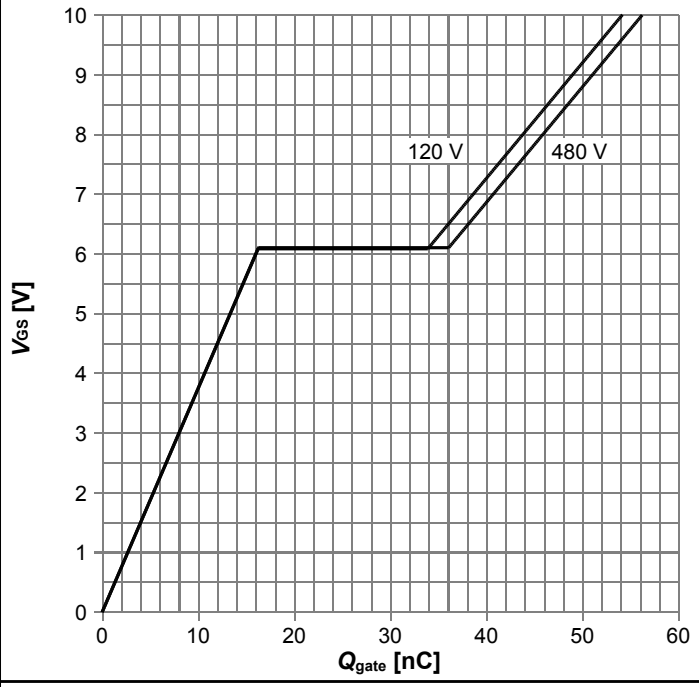
$R_{DS(on)}=f(T_j)$; $I_D=11.6$ A; $V_{GS}=10$ V

Diagram 13: Typ. transfer characteristics



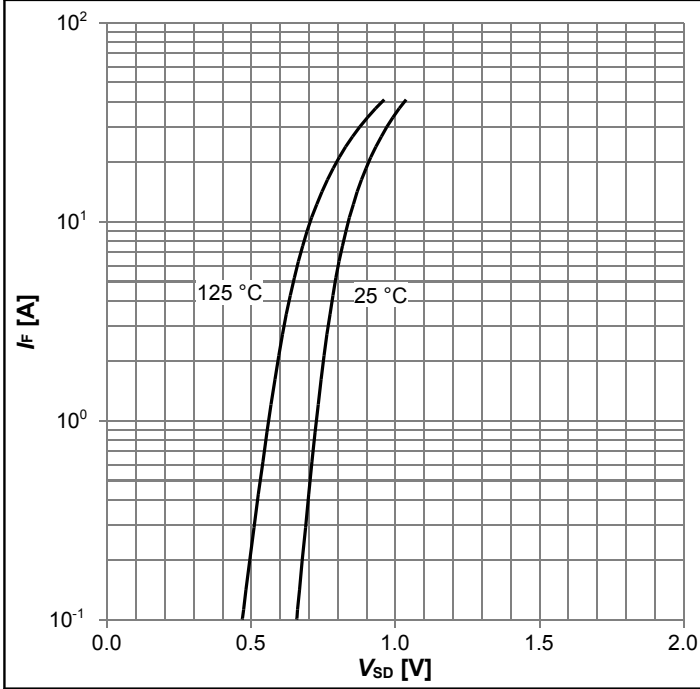
I_D=f(V_{GS}); V_{DS}=20V; parameter: T_j

Diagram 14: Typ. gate charge



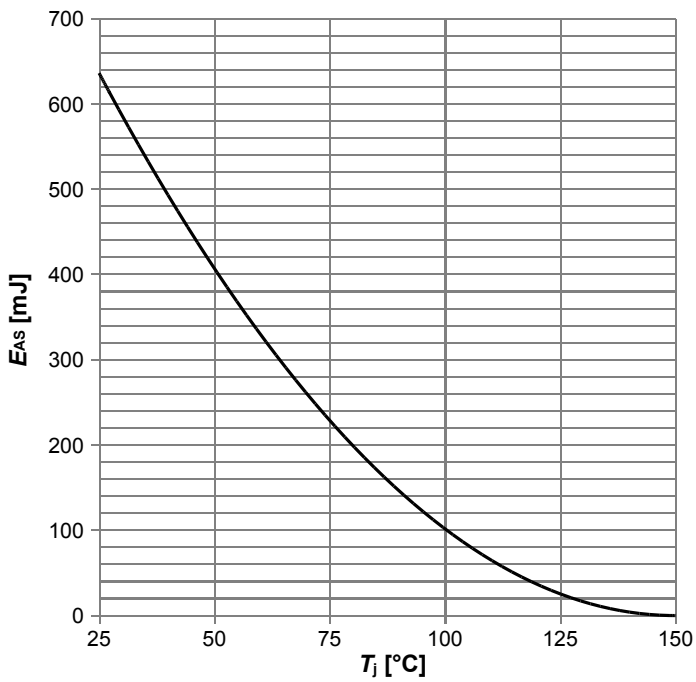
V_{GS}=f(Q_{gate}); I_D=14.5 A pulsed; parameter: V_{DD}

Diagram 15: Forward characteristics of reverse diode



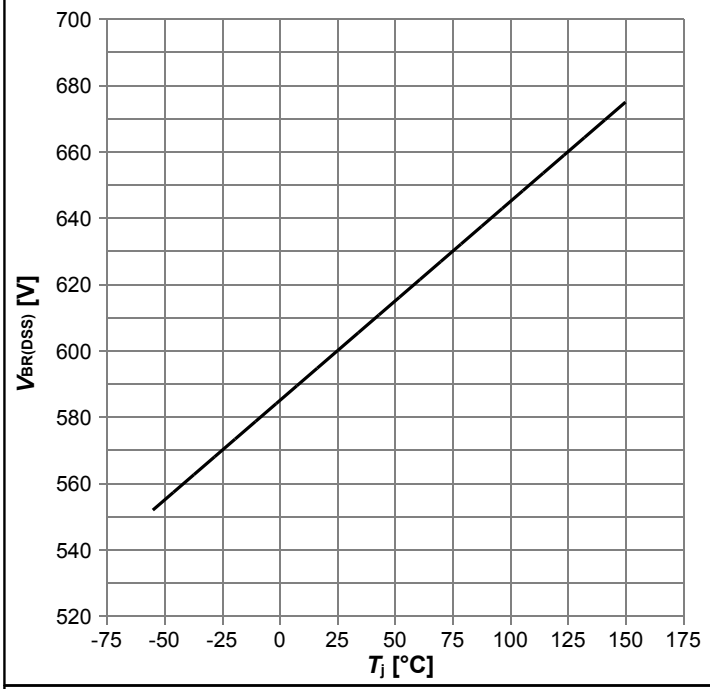
I_F=f(V_{SD}); parameter: T_j

Diagram 16: Avalanche energy



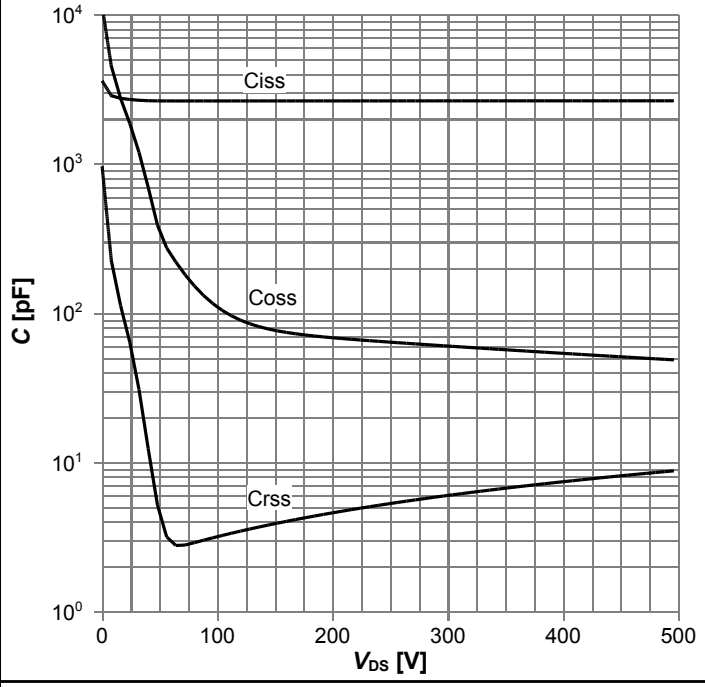
E_{AS}=f(T_j); I_D=5.2 A; V_{DD}=50 V

Diagram 17: Drain-source breakdown voltage



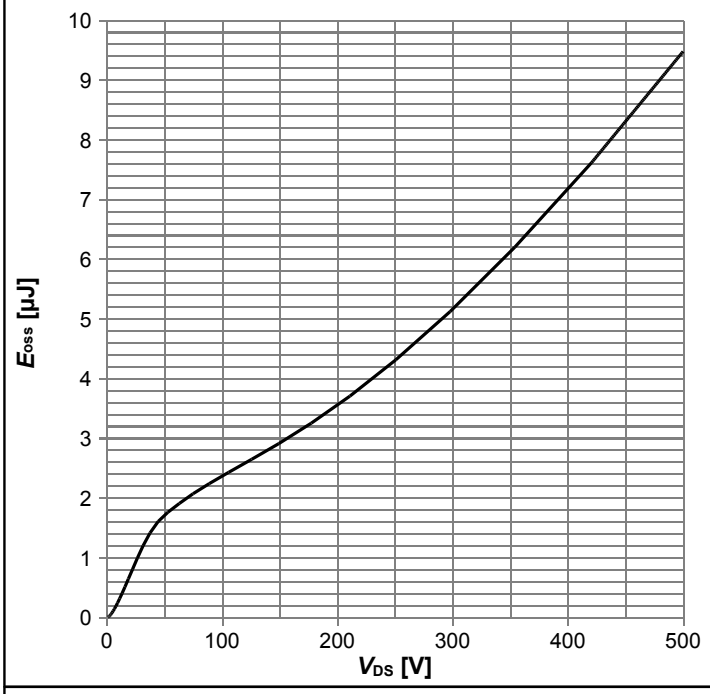
$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram 18: Typ. capacitances



C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 19: Typ. Coss stored energy



E_{oss}=f(V_{DS})

6 Test Circuits

Table 9 Diode characteristics

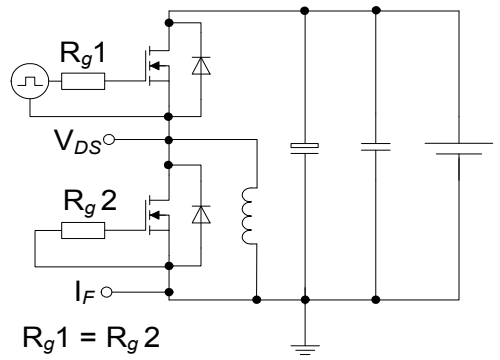
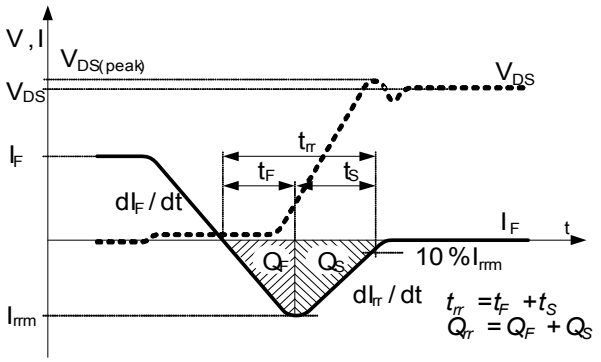
Test circuit for diode characteristics	Diode recovery waveform
	

Table 10 Switching times

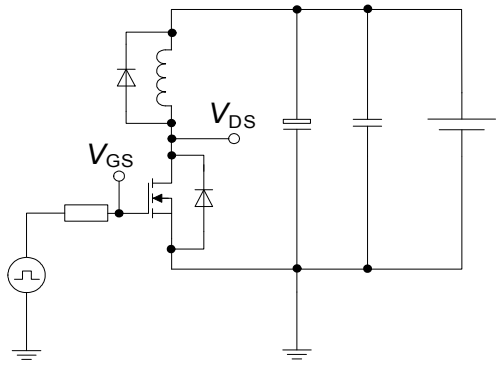
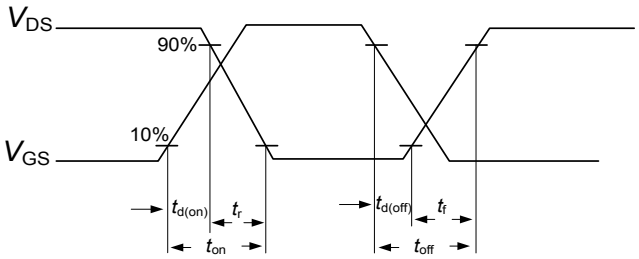
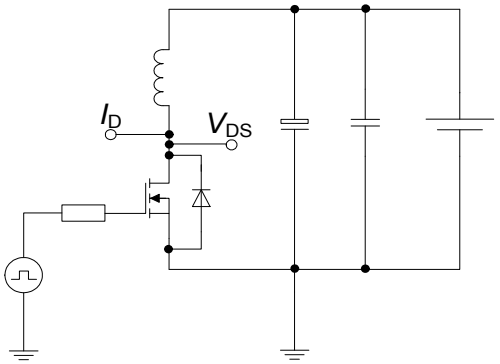
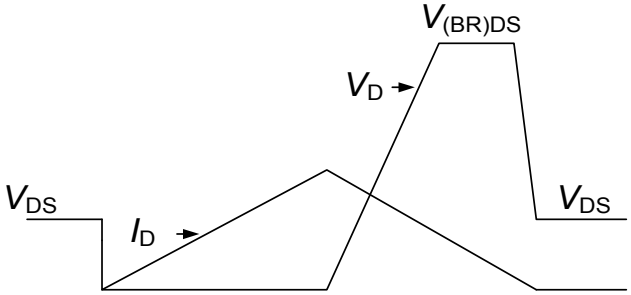
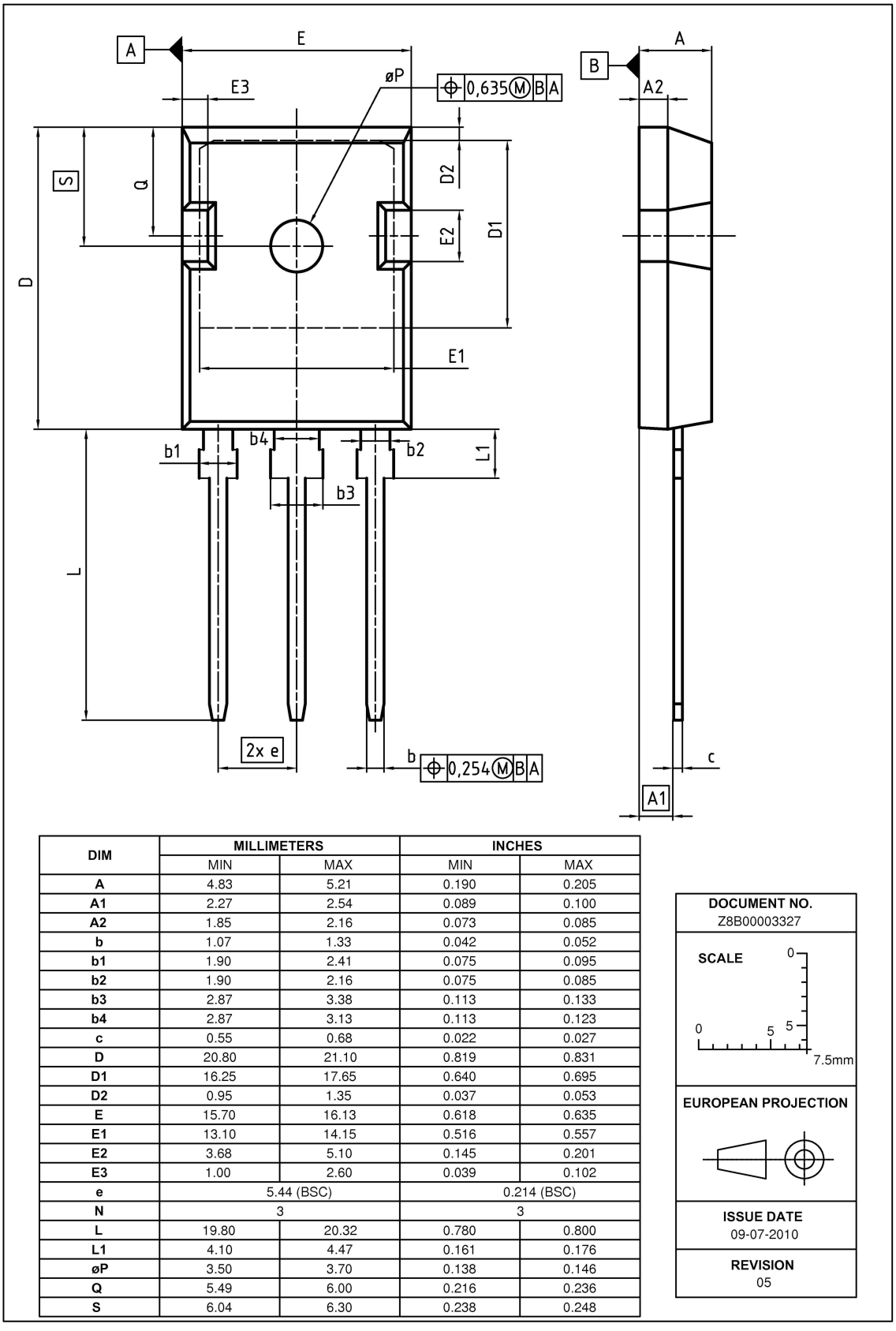
Switching times test circuit for inductive load	Switching times waveform
	

Table 11 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

7 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.83	5.21	0.190	0.205
A1	2.27	2.54	0.089	0.100
A2	1.85	2.16	0.073	0.085
b	1.07	1.33	0.042	0.052
b1	1.90	2.41	0.075	0.095
b2	1.90	2.16	0.075	0.085
b3	2.87	3.38	0.113	0.133
b4	2.87	3.13	0.113	0.123
c	0.55	0.68	0.022	0.027
D	20.80	21.10	0.819	0.831
D1	16.25	17.65	0.640	0.695
D2	0.95	1.35	0.037	0.053
E	15.70	16.13	0.618	0.635
E1	13.10	14.15	0.516	0.557
E2	3.68	5.10	0.145	0.201
E3	1.00	2.60	0.039	0.102
e	5.44 (BSC)		0.214 (BSC)	
N	3		3	
L	19.80	20.32	0.780	0.800
L1	4.10	4.47	0.161	0.176
øP	3.50	3.70	0.138	0.146
Q	5.49	6.00	0.216	0.236
S	6.04	6.30	0.238	0.248

DOCUMENT NO.
Z8B00003327

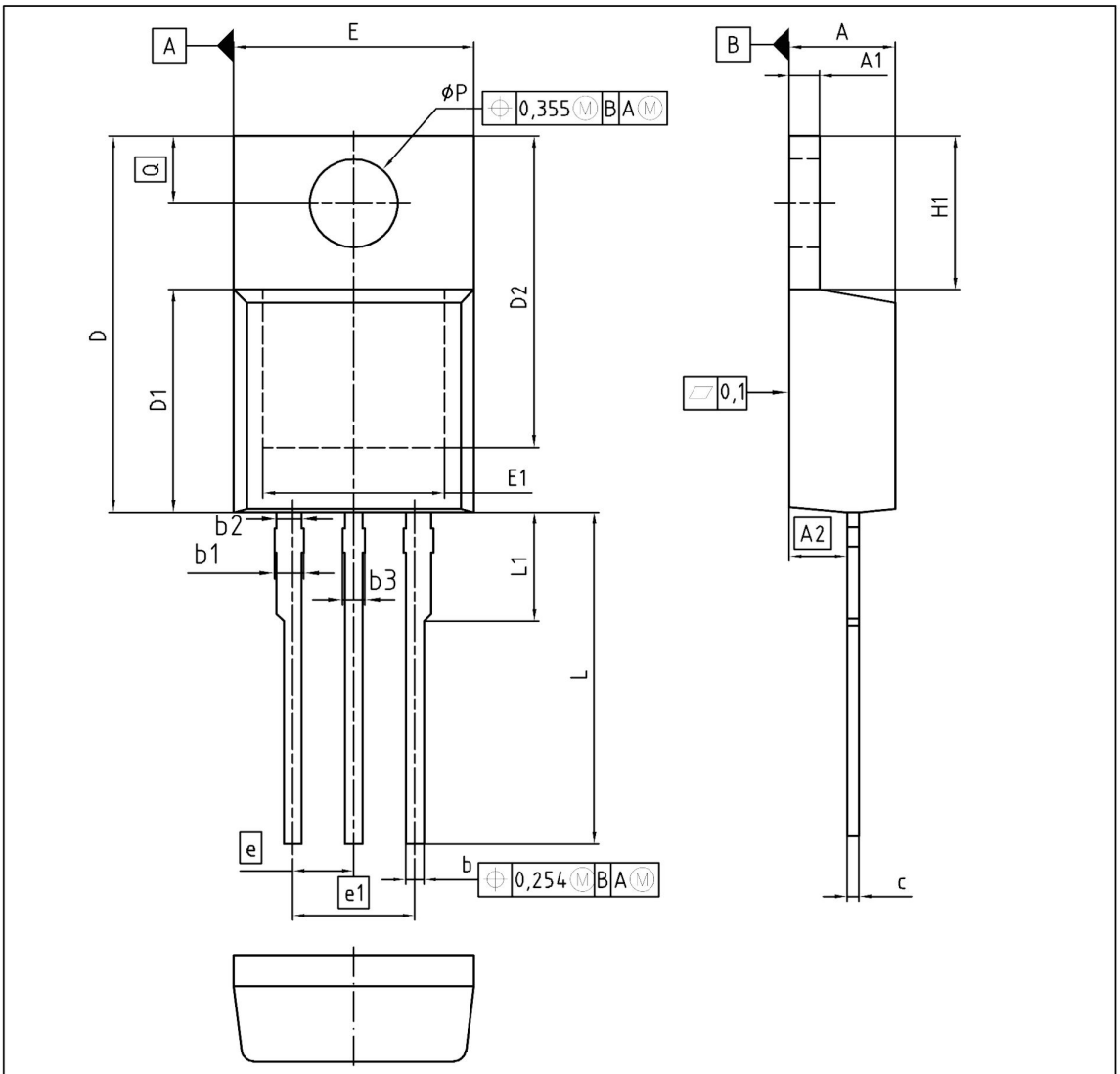
SCALE
0 5 5 7.5mm

EUROPEAN PROJECTION

ISSUE DATE
09-07-2010

REVISION
05

Figure 1 Outline PG-TO 247, dimensions in mm/inches



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	1.17	1.40	0.046	0.055
A2	2.15	2.72	0.085	0.107
b	0.65	0.86	0.026	0.034
b1	0.95	1.40	0.037	0.055
b2	0.95	1.15	0.037	0.045
b3	0.65	1.15	0.026	0.045
c	0.33	0.60	0.013	0.024
D	14.81	15.95	0.583	0.628
D1	8.51	9.45	0.335	0.372
D2	12.19	13.10	0.480	0.516
E	9.70	10.36	0.382	0.408
E1	6.50	8.60	0.256	0.339
e	2.54		0.100	
e1	5.08		0.200	
N	3		3	
H1	5.90	6.90	0.232	0.272
L	13.00	14.00	0.512	0.551
L1	-	4.80	-	0.189
øP	3.60	3.89	0.142	0.153
Q	2.60	3.00	0.102	0.118

DOCUMENT NO.
Z8B00003318

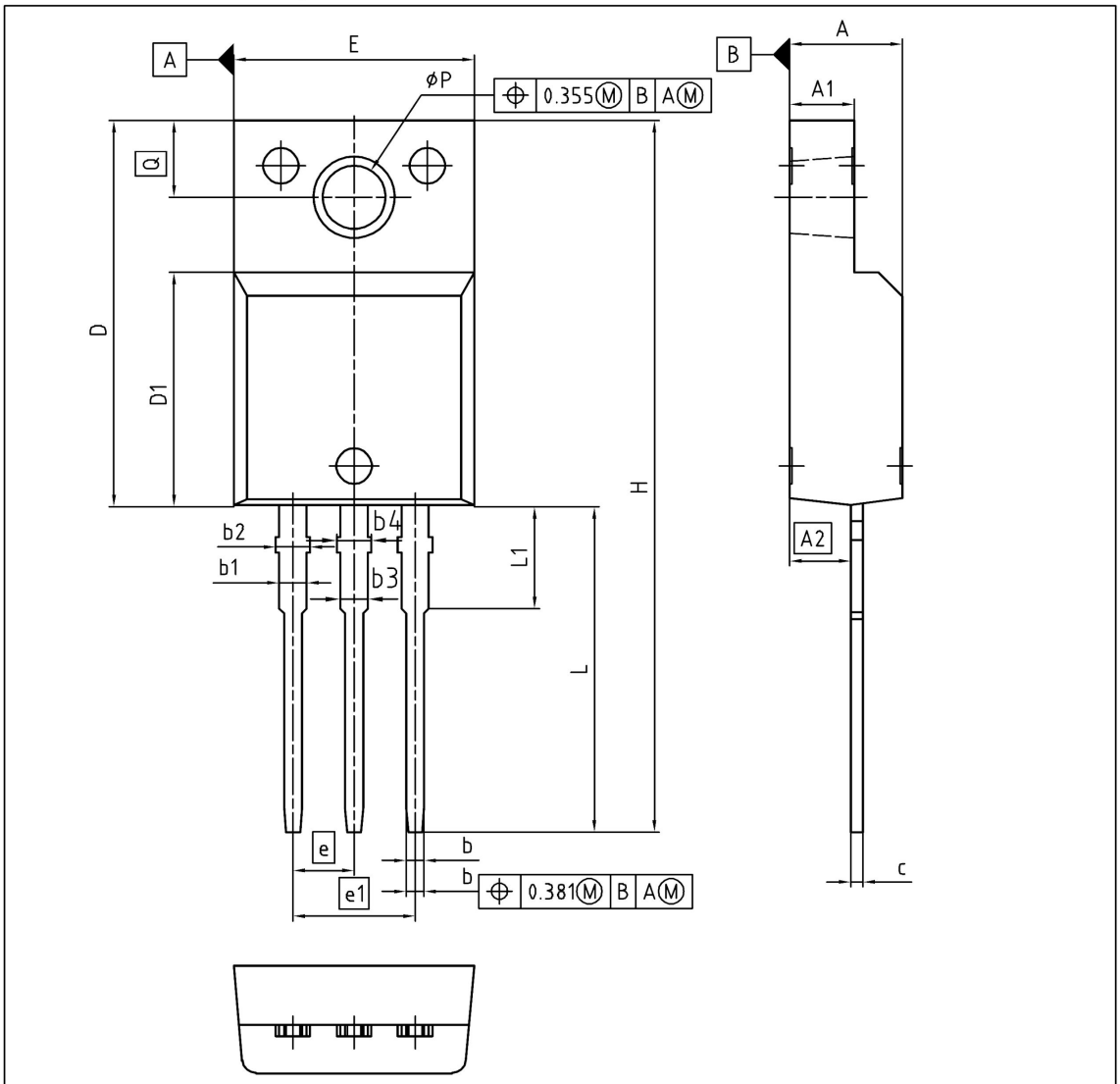
SCALE 0 2.5 0 2.5 5mm

EUROPEAN PROJECTION

ISSUE DATE
30-07-2009

REVISION
06

Figure 2 Outline PG-TO 220, dimensions in mm/inches



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.55	4.85	0.179	0.191
A1	2.55	2.85	0.100	0.112
A2	2.42	2.72	0.095	0.107
b	0.65	0.85	0.026	0.033
b1	0.95	1.33	0.037	0.052
b2	0.95	1.51	0.037	0.059
b3	0.65	1.33	0.026	0.052
b4	0.65	1.51	0.026	0.059
c	0.40	0.63	0.016	0.025
D	15.85	16.15	0.624	0.636
D1	9.53	9.83	0.375	0.387
E	10.35	10.65	0.407	0.419
e	2.54		0.100	
e1	5.08		0.200	
N	3		3	
H	29.45	29.75	1.159	1.171
L	13.45	13.75	0.530	0.541
L1	3.15	3.45	0.124	0.136
øP	2.95	3.20	0.116	0.126
Q	3.15	3.50	0.124	0.138

DOCUMENT NO.
Z8B00003319

SCALE 0 2.5 0 2.5 5mm

EUROPEAN PROJECTION

ISSUE DATE
08-03-2007

REVISION
03

Figure 3 Outline PG-TO 220 FullPAK, dimensions in mm/inches

8 Appendix A

Table 12 Related Links

- **IFX CoolMOS™ P6 Webpage:** www.infineon.com
- **IFX CoolMOS™ P6 application note:** www.infineon.com
- **IFX CoolMOS™ P6 simulation model:** www.infineon.com
- **IFX Design tools:** www.infineon.com

Revision History

IPW60R125P6, IPP60R125P6, IPA60R125P6

Revision: 2014-03-07, Rev. 2.0

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
2.0	2014-03-07	Release of final version

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Published by
Infineon Technologies AG
81726 München, Germany

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