Residual Phase Noise and Time Jitters of Single-Chip Digital Frequency Dividers

Lu-Lu Yan, Sen Meng, Wen-Yu Zhao, Wen-Ge Guo, Hai-Feng Jiang, and Shou-Gang Zhang

***Abstract*—In this paper, we demonstrate the residual phase noise of a few microwave frequency dividers which usually limit the performance of frequency synthesizers. In order to compare these dividers under different operation frequencies, we calculate additional time jitters of these dividers by using the measured phase noise. The time jitters are various from ~0.1 fs to 43 fs in a bandwidth from 1 Hz to 100 Hz in dependent of models and operation frequencies. The HMC series frequency dividers exhibit outstanding performance for high operation frequencies, and the time jitters can be sub-fs. The time jitters of SP8401, MC10EP139, and MC100LVEL34 are comparable or even below that of HMC series for low operation frequencies.**

***Index Terms*—Frequency divider, phase noise, spectra analysis, time jitter.**

1. Introduction

Frequency synthesizers are widely used in modern electronic systems and their near carrier offset phase noise is often critical to many applications. Most synthesizers are of the phase-locked type, employing frequency multipliers or frequency dividers to convert frequencies[1],[2]. Usually, noise introduced by passive components is negligible, and frequency multipliers or frequency dividers limit the performance of these synthesizers. In comparison with frequency multipliers, frequency dividers are more flexible to use with plenty of chooses. A hybrid frequency divider, composed of a digital divider and a regenerative divider, converts an 8 GHz signal to 5 MHz with time jitters about 6 fs in a bandwidth of 1 Hz to 100 Hz and about 40 fs in a bandwidth of 1 Hz to 100 kHz[3]. This result is comparable with the best frequency multiplier named nonlinear transmission line (NLTL)[4],[5] which is not commercially available any more.

The regenerative frequency divider exhibits the lowest additional phase noise for low frequency operation, the additional jitter (160 MHz to 5 MHz) in the bandwidth from 1 Hz to 100 Hz is about 5 fs[3]. However, the regenerative frequency divider is bulky and expensive. Digital logic units, such as complex programmable logic device (CPLD) and field programmable gate array (FPGA), can easily realize programmable frequency-dividing. However, the additional noise of CPLD and FPGA is high[6]. In order to have a simple and compact low-noise synthesizer, the single-chip digital frequency divider seems to be the best solution. Unfortunately, manufactures of these chips do not provide the near carrier additional phase noise of their products.

In this paper, we show the residual phase noise and additional time jitters of six models of digital frequency dividers made by three companies (Onsemi, Zarlink, and Hittite). At low frequencies, the residual phase noise follows $1/f$ rules in general, where f is frequency. The time jitters are given for comparing additional noise level induced by these frequency dividers in different frequencies.

2. Experimental Setup and Measurement Results

Fig. 1 shows the experimental setup. We drive two identical digital frequency dividers under test (DUT) with a common reference source. RF/MW amplifiers are used to produce about 10 dBm to 19 dBm frequency-divided signals. After DUT, a low-pass filter is used to pick up the necessary signals. The phase detector is a 7 dBm level mixer which gives the phase difference variation. A phase shifter is employed to establish the quadrature phase (90°) between two DUT signals at the mixer inputs. The signal out from the mixer IF port is transmitted to a dynamic

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signal analyzer, also called fast Fourier transmitter (FFT), via a low-pass filter and low noise baseband amplifier. In this measurement system, the mixer and amplifier convert a phase fluctuation to a voltage change with a conversion factor of about 9.7 V/rad.

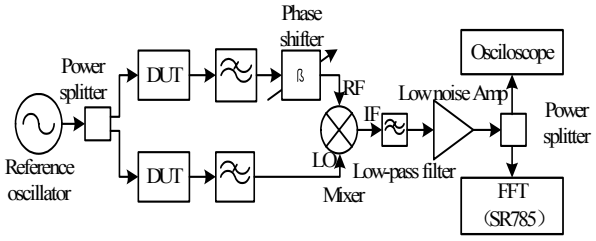

Fig. 1. Phase noise measurement experimental setup, DUT: Digital-frequency-divider under test.

We choose six digital frequency dividers, including SP 8401, MC10EP139[7], MC100LVEL34[8], HMC361[9], HMC362[10], and HMC363[11]. Although the datasheets of these dividers often claim only the maximum operation frequency, these dividers do not work normally when the input frequency below a certain threshold. SP8401 operates only in relative low frequencies ranging from 50 MHz to 300 MHz; MC10EP139 and MC100LVEL34 can work up to 1 GHz; HMC series dividers run well over 10 GHz. We design a PCB layout by putting these discrete components in a large space for avoiding stray effects.

Fig. 2 to Fig. 7 show the residual double sideband phase noise of corresponding frequency dividers. These data have been reduced 3 dB from the FFT measured data to represent the noise of a single divider. In this experiment, the input operating frequencies are listed in the Table 1. The output power of the common reference source is 3 dBm. We add attenuators behind the low-pass filter, in order to ensure that the input power at the mixer's LO port is about 8 dBm and –1 dBm at the RF port.

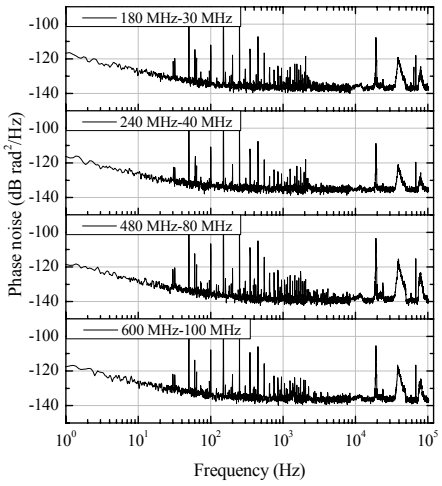

Fig. 2. Residual double-sideband (DSB) phase noise of the MC10EP139 with different operation frequencies.

Note that the measured phase noise also includes noise induced by the RF/MW amplifiers and measurement system. Especially at low operation frequencies, the measurement noise is not negligible. Noise spurs shown in these figures are attributed to the power supply.

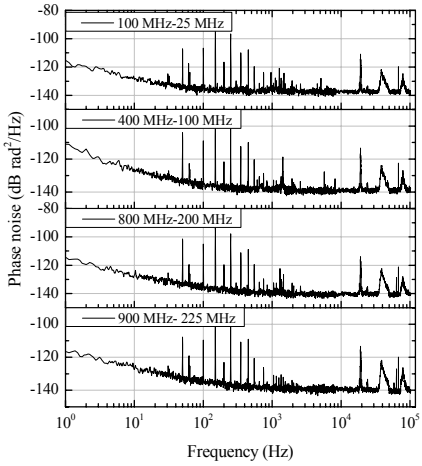

Fig. 3. Residual DSB phase noise of the MC100LVEL34.

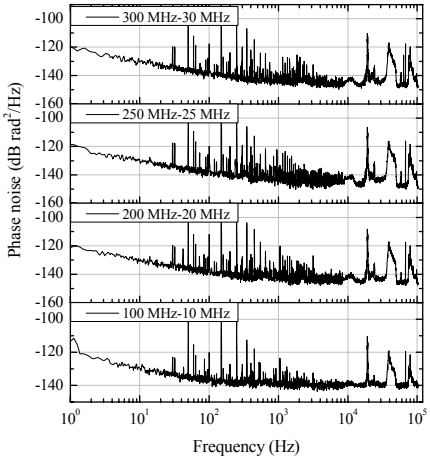

Fig. 4. Residual DSB phase noise of the SP8401.

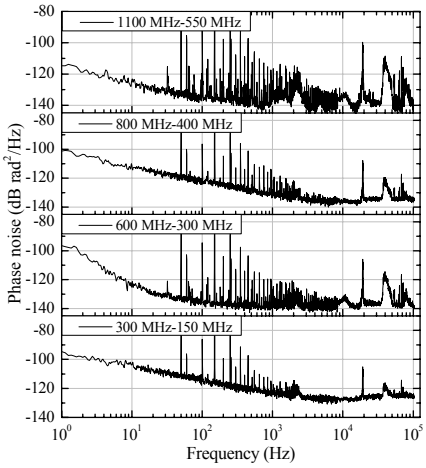

Fig. 5. Residual DSB phase noise of the HMC361.

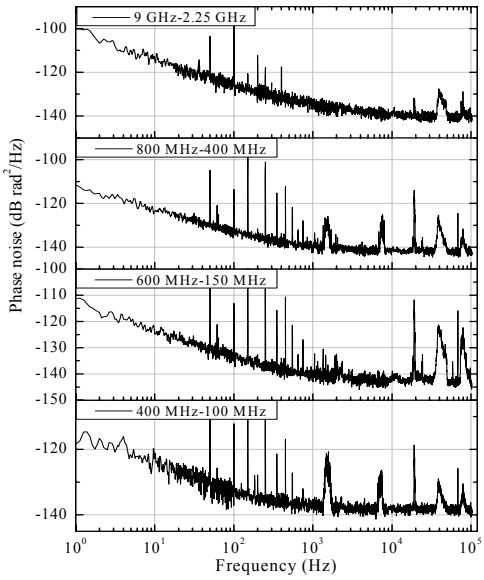

Fig. 6. Residual DSB phase noise of the HMC362.

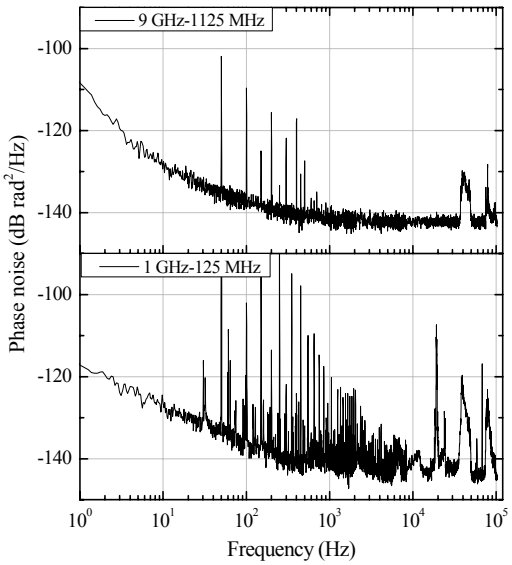

Fig. 7. Residual DSB phase noise of the HMC363.

Table 1: Measured phase noise and calculated time jitters
(Note that noise introduced by RF/MW amplifiers and measurement system is included.)

Divider	Function	Input frequency range (GHz)	Input/output frequency (MHz)	Time jitter in 1 Hz to 100 Hz (fs)	Additional DSB phase noise@1 Hz (dB rad²/Hz)	Additional time jitter@1 Hz (fs/$\sqrt{\text{Hz}}$)
MC10EP139	÷2/4,÷4/5/6	0.01 to 1	180/30	18.00	–117	7.80
			240/40	14.00	–116	6.10
			480/80	6.50	–119	2.40
			600/100	6.20	–118	2.10
MC100LVEL34	÷2/4/8	0.01 to 1.5	100/25	19.00	–115	11.00
			400/100	6.30	–111	4.50
			800/200	2.70	–114	1.50
			900/225	2.50	–116	1.10
SP8401	÷10/11	0.05 to 0.3	100/10	43.00	–113	34.00
			200/20	19.00	–121	6.90
			250/25	15.00	–119	7.50
			300/30	12.00	–120	5.60
HMC361S8G	÷2	0.3 to 10	300/150	43.00	–95	20.00
			600/300	7.60	–97	7.80
			800/400	6.90	–101	3.50
			1100/550	0.12	–115	0.53
HMC362S8G	÷4	0.1 to 12	400/100	7.10	–112	1.90
			600/150	5.10	–113	2.90
			800/200	4.00	–114	2.10
			9000/2250	1.10	–99	0.70
HMC363S8G	÷8	0.3 to 12	1000/125	4.00	–117	1.80
			9000/1125	0.53	–108	0.54

It is not easy to compare these curves directly because the frequencies are different. We calculate the time jitters as shown in Table 1 without considering the noise spurs[12], so as to give a quick comparison of these dividers. The computational formula is given by

$$T_j = \sqrt{\int_{f_1}^{f_2} S_\varphi(f)\,df} \Big/ 2\pi f \tag{1}$$

where T_j is the time jitter, f_2 and f_1 are the up and down

limit, respectively. $S_\varphi(f)$ is the phase noise power spectra density, and f is the output frequency of the dividers under test. The operation frequency range is obtained by a quick test. We tune the input frequency and monitor the output of these dividers. When the input frequency is below a certain value (lower operation frequency), the output of these dividers becomes very noisy. The lower operation frequencies may change the dependence on the surrounding circuits. However, it has never been close to DC as indicated in these datasheets.

SP8401 made by Zarlink is an old produce with a CMOS and TTL compatible level. MC10EP139 and MC100LV EL34 made by Onsemi have an emitter coupled logic (ECL) input/output level. The wafer process of these two dividers is MOSAIC5 of Onsemi. MOSAIC5 is a trench isolated, double epi, double poly, and multi-layer metal, it has a minimum photolithography feature size of 0.7 μm. Additionally, MOSAIC5 utilizes an industry standard inorganic interlayer dielectric layer. HMC series frequency dividers made by Hittite employes the GaAs HBT-A wafer process. The InGaP GaAs HBT has an ultra-fast response, and the operation frequencies of these HBTs can be up to 60 GHz.

3. Conclusions

In this work, we have measured the phase noise and time jitters of six digital frequency dividers. Generally, the time jitter is lower while the operation frequency is higher, and a high speed digital frequency divider exhibits lower additional time jitter. HMC series frequency dividers, with InGaP GaAs heterojunction bipolar transistors (HBT) technology, exhibit outstanding performance for high operation frequencies; the time jitter can be sub-fs. The time jitter in a bandwidth of 1 Hz to 100 Hz is in the range of 0.1 fs to 43 fs dependent on the operation frequency and divider model. In comparison with dividers realized with the CPLD or FPGA, single-chip digital frequency dividers have lower additional noise.

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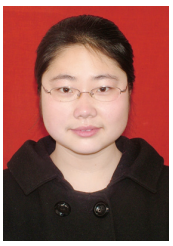

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